

TC74HC175AP, TC74HC175AF, TC74HC175AFN

Quad D-Type Flip Flop with Clear

The TC74HC175A is a high speed CMOS D-TYPE FLIP FLOP fabricated with silicon gate C2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Information signals applied to D inputs are transferred to the Q and \bar{Q} outputs on the positive going edge of the clock pulse.

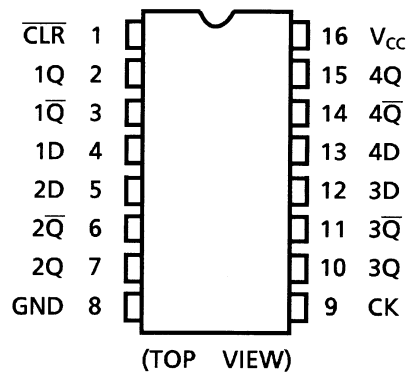
When the $\overline{\text{CLR}}$ input is held low, the Q outputs are at the low logic level and the \bar{Q} outputs are at the high logic level independent of the other inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

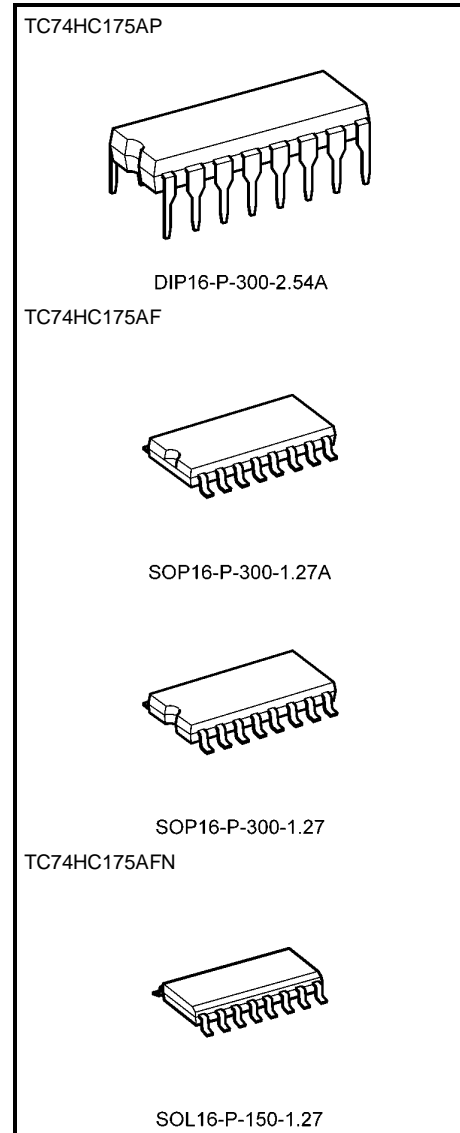
Features

- High speed: $f_{\text{max}} = 63 \text{ MHz (typ.)}$ at $V_{\text{CC}} = 5 \text{ V}$
- Low power dissipation: $I_{\text{CC}} = 4 \mu\text{A (max)}$ at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC (min)}}$
- Symmetrical output impedance: $|I_{\text{OH}}| = I_{\text{OL}} = 4 \text{ mA (min)}$
- Balanced propagation delays: $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Wide operating voltage range: $V_{\text{CC (opr)}} = 2 \text{ to } 6 \text{ V}$
- Pin and function compatible with 74LS175

Pin Assignment

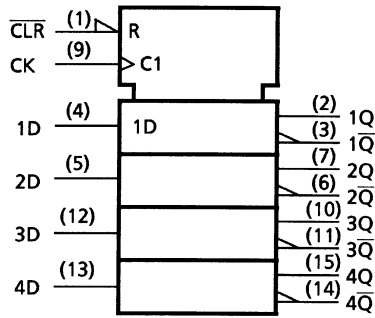


Note: xxxFN (JEDEC SOP) is not available in Japan.



Weight	
DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)
SOP16-P-300-1.27	: 0.18 g (typ.)
SOL16-P-150-1.27	: 0.13 g (typ.)

IEC Logic Symbol

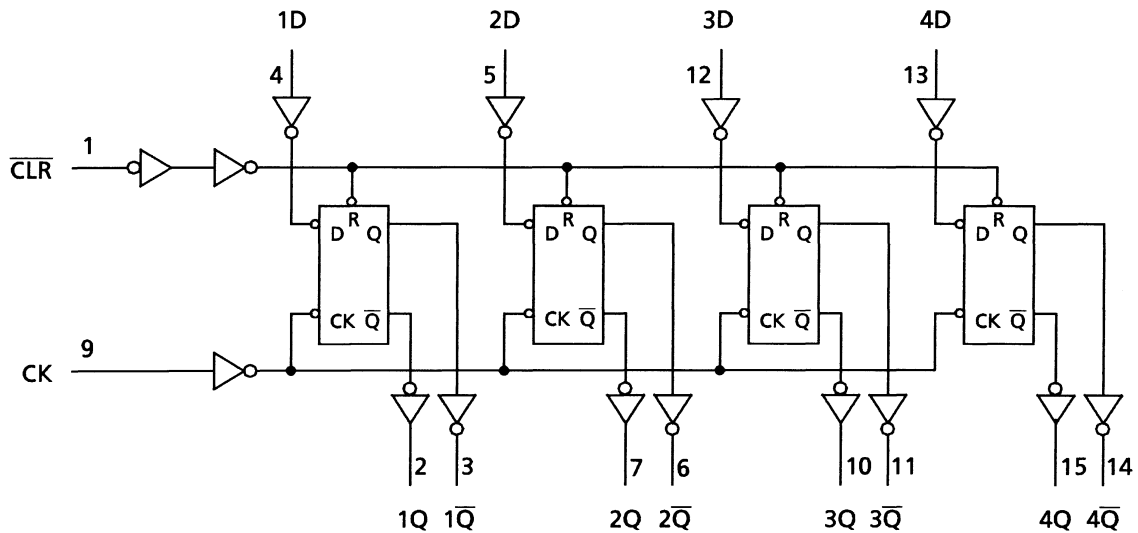


Truth Table

Inputs			Outputs		Function
CLR	D	CK	Q	\bar{Q}	
L	X	X	L	H	Clear
H	L	\uparrow	L	H	—
H	H	\uparrow	H	L	—
H	X	\downarrow	Q_n	\bar{Q}_n	No Change

X: Don't care

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7	V
DC input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 50	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Note 2: 500 mW in the range of $T_a = -40$ to $65^{\circ}C$. From $T_a = 65$ to $85^{\circ}C$ a derating factor of -10 mW/ $^{\circ}C$ shall be applied until 300 mW.

Recommended Operating Conditions (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	$^{\circ}C$
Input rise and fall time	t_r, t_f	0 to 1000 ($V_{CC} = 2.0$ V) 0 to 500 ($V_{CC} = 4.5$ V) 0 to 400 ($V_{CC} = 6.0$ V)	ns

Note: The recommended operating conditions are required to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V _{CC} (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V _{IH}	—		2.0	1.50	—	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	
				6.0	4.20	—	—	4.20	—	
Low-level input voltage	V _{IL}	—		2.0	—	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
			I _{OH} = -4 mA	4.5	4.18	4.31	—	4.13	—	
				6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
			I _{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	
				6.0	—	0.18	0.26	—	0.33	
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		6.0	—	—	4.0	—	40.0	μA

Timing Requirements (input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C		Unit
			V _{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width (CK)	t_W (L) t_W (H)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ($\overline{\text{CLR}}$)	t_W (L)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time	t_s	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum hold time	t_h	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum removal time	t_{rem}	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Clock frequency	f	—	2.0	—	6	5	MHz
			4.5	—	31	25	
			6.0	—	36	29	

AC Characteristics ($C_L = 15 \text{ pF}$, $V_{CC} = 5 \text{ V}$, $T_a = 25^\circ\text{C}$, input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH}	—	—	4	8	ns
	t_{THL}					
Propagation delay time (CK-Q, \overline{Q})	t_{pLH}	—	—	16	24	ns
	t_{pHL}					
Propagation delay time ($\overline{\text{CLR}}$ -Q, \overline{Q})	t_{pLH}	—	—	13	21	ns
	t_{pHL}					
Maximum clock frequency	f_{max}	—	36	63	—	MHz

AC Characteristics ($C_L = 50 \text{ pF}$, input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C				Ta = -40 to 85°C		Unit
			VCC (V)	Min	Typ.	Max	Min	Max	
Output transition time	t_{TLH} t_{THL}	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time (CK-Q, \bar{Q})	t_{pLH} t_{pHL}	—	2.0	—	70	140	—	175	ns
			4.5	—	19	28	—	35	
			6.0	—	16	24	—	30	
Propagation delay time (\bar{CLR} -Q, \bar{Q})	t_{pLH} t_{pHL}	—	2.0	—	50	125	—	160	ns
			4.5	—	16	25	—	32	
			6.0	—	12	22	—	27	
Maximum clock frequency	f_{max}	—	2.0	6	14	—	5	—	MHz
			4.5	31	53	—	25	—	
			6.0	36	63	—	29	—	
Input capacitance	C_{IN}	—	—	5	10	—	10	pF	
Power dissipation capacitance	C_{PD} (Note)	—	—	53	—	—	—	pF	

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC} (\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per F/F)}$$

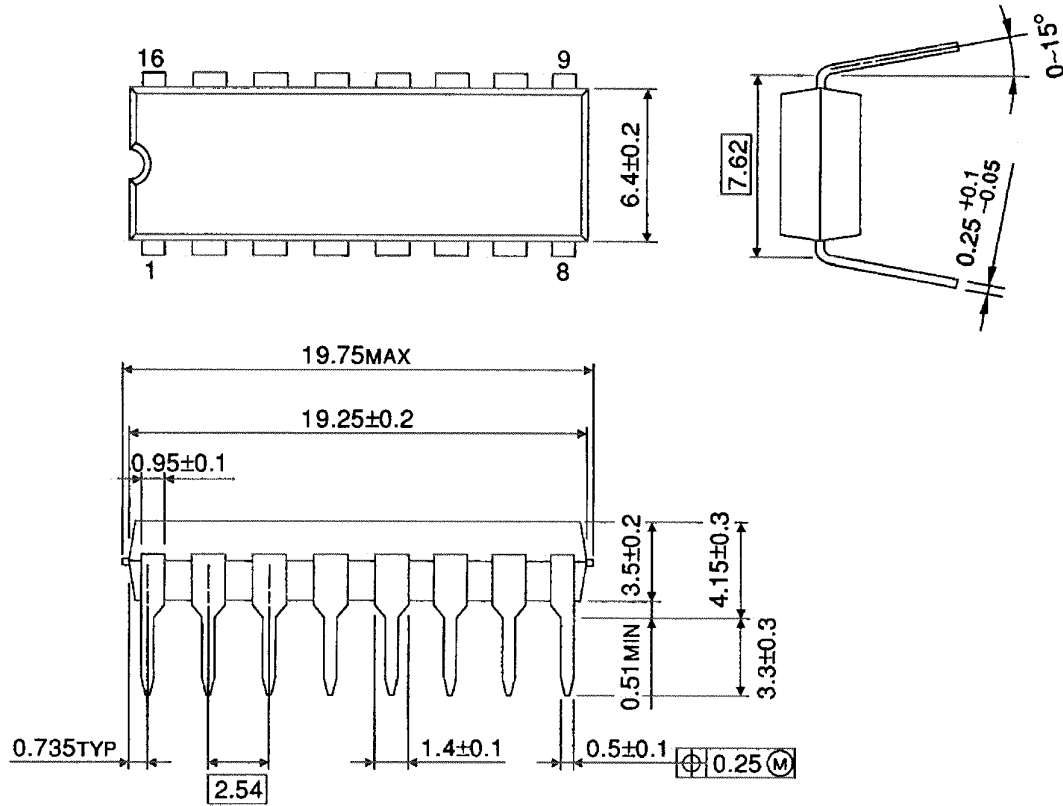
And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:

$$C_{PD} (\text{total}) = 32 + 21 \cdot n$$

Package Dimensions

DIP16-P-300-2.54A

Unit : mm

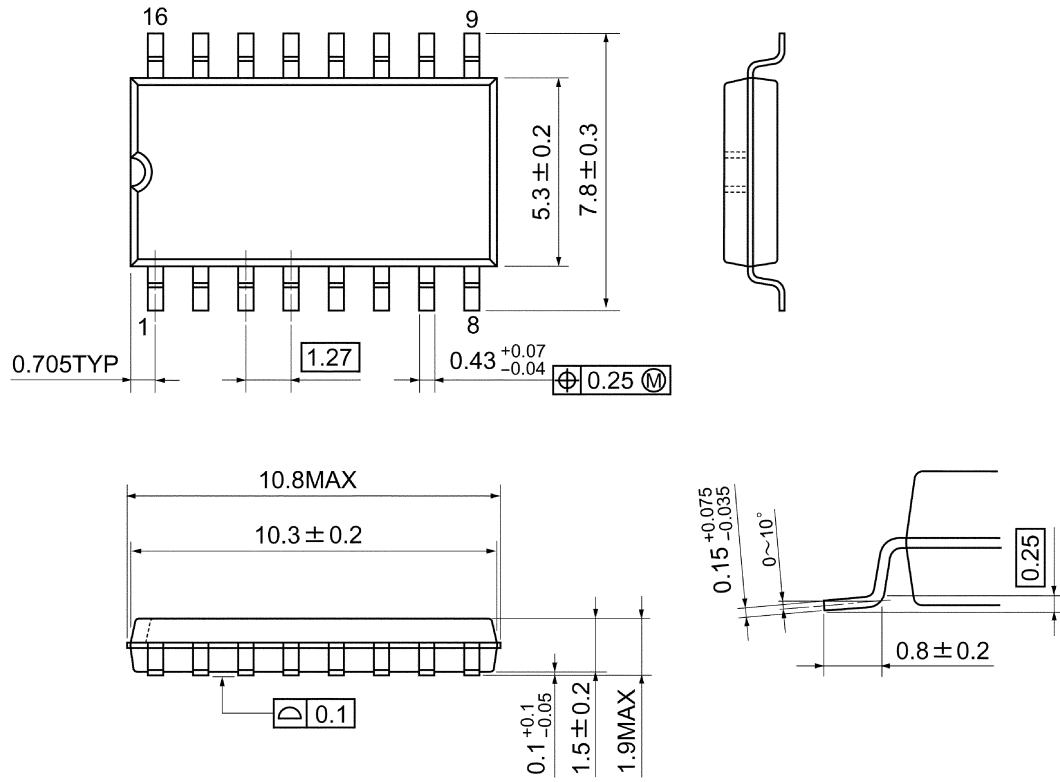


Weight: 1.00 g (typ.)

Package Dimensions

SOP16-P-300-1.27A

Unit: mm

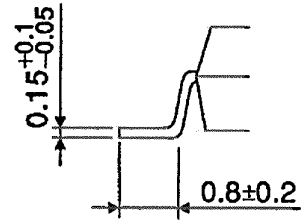
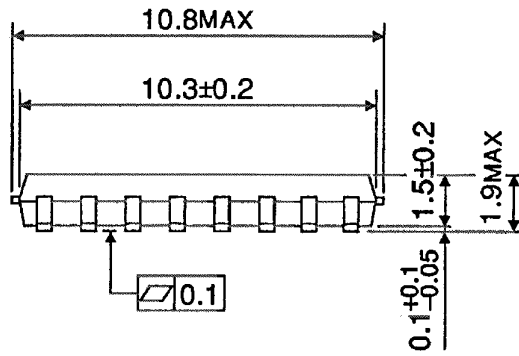
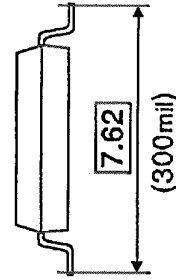
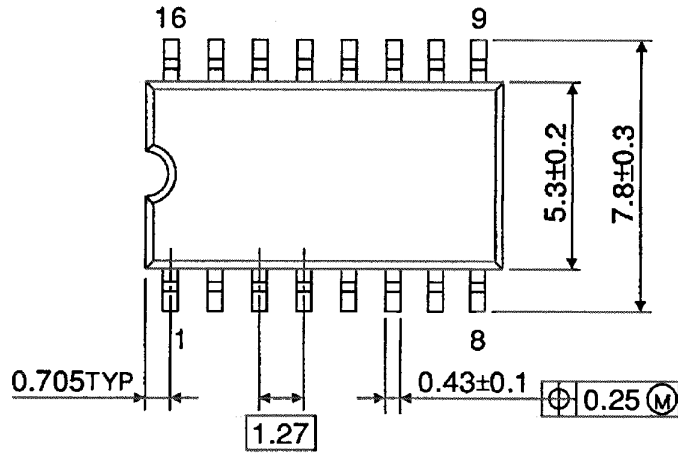


Weight: 0.18 g (typ.)

Package Dimensions

SOP16-P-300-1.27

Unit : mm

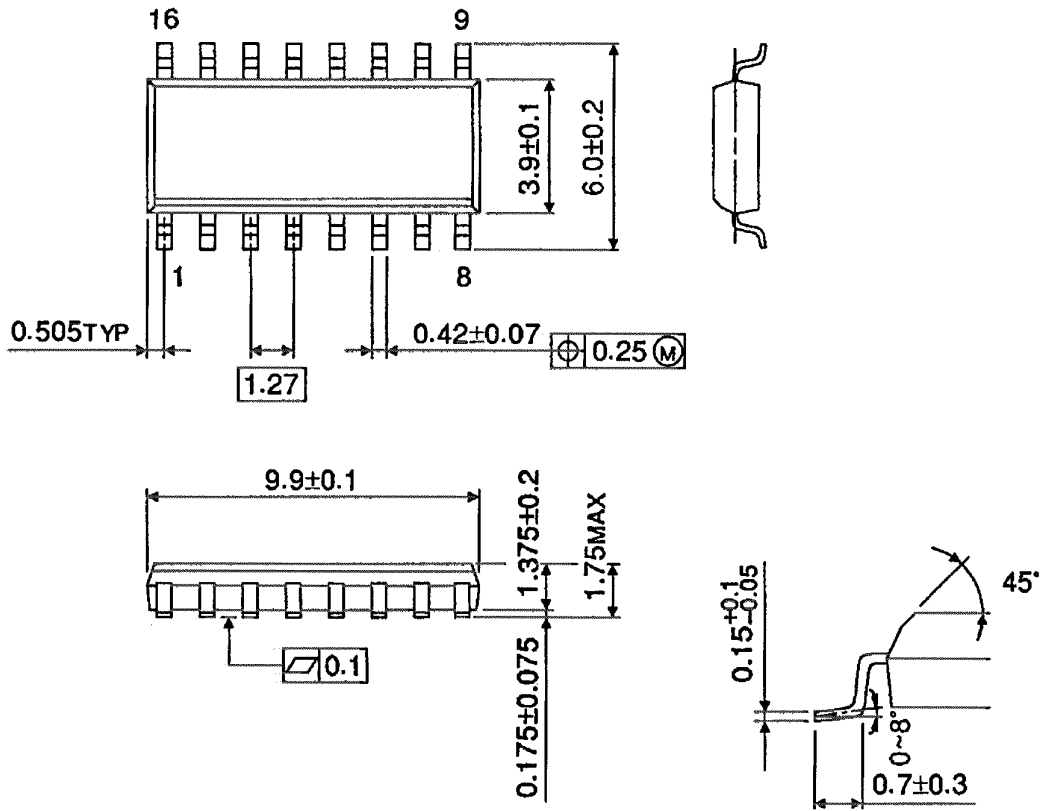


Weight: 0.18 g (typ.)

Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

Note: Lead (Pb)-Free Packages**DIP16-P-300-2.54A SOP16-P-300-1.27A SOL16-P-150-1.27****RESTRICTIONS ON PRODUCT USE**

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