

LMH6550

Differential, High Speed Op Amp

General Description

The LMH[®]6550 is a high performance voltage feedback differential amplifier. The LMH6550 has the high speed and low distortion necessary for driving high performance ADCs as well as the current handling capability to drive signals over balanced transmission lines like CAT 5 data cables. The LMH6550 can handle a wide range of video and data formats.

With external gain set resistors, the LMH6550 can be used at any desired gain. Gain flexibility coupled with high speed makes the LMH6550 suitable for use as an IF amplifier in high performance communications equipment.

The LMH6550 is available in the space saving SOIC and MSOP packages.

Features

- 400 MHz -3 dB bandwidth ($V_{OUT} = 0.5 V_{PP}$)
- 90 MHz 0.1 dB bandwidth
- 3000 V/ μ s slew Rate
- 8 ns settling time to 0.1%
- -92/-103 dB HD2/HD3 @ 5 MHz
- 10 ns shutdown/enable

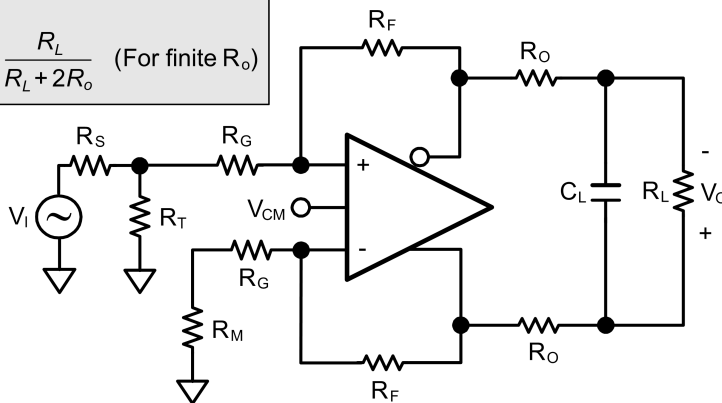
Applications

- Differential AD driver
- Video over twisted pair
- Differential line driver
- Single end to differential converter
- High speed differential signaling
- IF/RF amplifier
- SAW filter buffer/driver

Typical Application

$$\frac{V_o}{V_i} = \frac{R_F}{2R_G} \quad (\text{For } R_o = 0\Omega)$$

$$\frac{V_o}{V_i} = \frac{R_F}{2R_G} \cdot \frac{R_L}{R_L + 2R_o} \quad (\text{For finite } R_o)$$



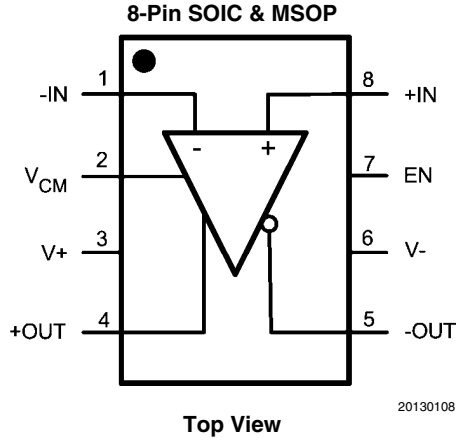
$$\text{SET } R_M = R_T || R_S$$

$$\text{SET } R_T = \frac{1}{\left(\frac{1}{R_S} - \frac{1}{R_{IN}}\right)}$$

$$R_{IN} = \frac{R_G}{1 - \left(\frac{R_F}{2 * (R_F + R_G)}\right)}$$

20130136

Connection Diagram



Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LMH6550MA	LMH6550MA	95/Rails	M08A
	LMH6550MAX		2.5k Units Tape and Reel	
8-Pin MSOP	LMH6550MM	AL1A	1k Units Tape and Reel	MUA08A
	LMH6550MMX		3.5k Units Tape and Reel	

Absolute Maximum Ratings *(Note 1)*

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance <i>(Note 5)</i>	
Human Body Model	2000V
Machine Model	200V
Supply Voltage	13.2V
Common Mode Input Voltage	$\pm V_S$
Maximum Input Current (pins 1, 2, 7, 8)	30 mA
Maximum Output Current (pins 4, 5)	<i>(Note 3)</i>
Maximum Junction Temperature	150°C

Soldering Information:

See Product Folder at www.national.com and <http://www.national.com/ms/MS/MS-SOLDERING.pdf>

Operating Ratings *(Note 1)*

Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Total Supply Voltage	4.5V to 12V
Package Thermal Resistance (θ_{JA}) <i>(Note 4)</i>	
8-Pin SOIC	150°C/W
8-Pin MSOP	235°C/W

$\pm 5V$ Electrical Characteristics *(Note 2)*

Single ended in differential out, $T_A = 25^\circ\text{C}$, $V_S = \pm 5V$, $V_{CM} = 0V$, $R_F = R_G = 365\Omega$, $R_L = 500\Omega$; Unless specified. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min <i>(Note 8)</i>	Typ <i>(Note 7)</i>	Max <i>(Note 8)</i>	Units
AC Performance (Differential)						
SSBW	Small Signal -3 dB Bandwidth	$V_{OUT} = 0.5 V_{PP}$		400		MHz
LSBW	Large Signal -3 dB Bandwidth	$V_{OUT} = 2 V_{PP}$		380		MHz
	Large Signal -3 dB Bandwidth	$V_{OUT} = 4 V_{PP}$		320		MHz
	0.1 dB Bandwidth	$V_{OUT} = 0.5 V_{PP}$		90		MHz
	Slew Rate	4V Step <i>(Note 6)</i>	2000	3000		V/ μs
	Rise/Fall Time	2V Step		1		ns
	Settling Time	2V Step, 0.1%		8		ns
V_{CM} Pin AC Performance (Common Mode Feedback Amplifier)						
	Common Mode Small Signal Bandwidth	V_{CM} Bypass Capacitor Removed		210		MHz
	Slew Rate	V_{CM} Bypass Capacitor Removed		200		V/ μs
Distortion and Noise Response						
HD2	2 nd Harmonic Distortion	$V_O = 2 V_{PP}$, $f = 5 \text{ MHz}$, $R_L = 800\Omega$		-92		dBc
		$V_O = 2 V_{PP}$, $f = 20 \text{ MHz}$, $R_L = 800\Omega$		-78		
		$V_O = 2 V_{PP}$, $f = 70 \text{ MHz}$, $R_L = 800\Omega$		-59		
HD3	3 rd Harmonic Distortion	$V_O = 2 V_{PP}$, $f = 5 \text{ MHz}$, $R_L = 800\Omega$		-103		dBc
		$V_O = 2 V_{PP}$, $f = 20 \text{ MHz}$, $R_L = 800\Omega$		-88		
		$V_O = 2 V_{PP}$, $f = 70 \text{ MHz}$, $R_L = 800\Omega$		-50		
e_n	Input Referred Voltage Noise	$f \geq 1 \text{ MHz}$		6.0		nV/ $\sqrt{\text{Hz}}$
i_n	Input Referred Noise Current	$f \geq 1 \text{ MHz}$		1.5		pA/ $\sqrt{\text{Hz}}$
Input Characteristics (Differential)						
V_{OSD}	Input Offset Voltage	Differential Mode, $V_{ID} = 0$, $V_{CM} = 0$		1	± 4 ± 6	mV
	Input Offset Voltage Average Temperature Drift	<i>(Note 10)</i>		1.6		$\mu\text{V}/^\circ\text{C}$
I_{BI}	Input Bias Current	<i>(Note 9)</i>	0	-8	-16	μA
	Input Bias Current Average Temperature Drift	<i>(Note 10)</i>		9.6		nA/ $^\circ\text{C}$
	Input Bias Difference	Difference in Bias Currents Between the Two Inputs		0.3		μA
CMRR	Common Mode Rejection Ratio	DC, $V_{CM} = 0V$, $V_{ID} = 0V$	72	82		dBc
R_{IN}	Input Resistance	Differential		5		M Ω

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
C_{IN}	Input Capacitance	Differential		1		pF
CMVR	Input Common Mode Voltage Range	CMRR > 53 dB	+3.1 -4.6	+3.2 -4.7		V
V_{CM} Pin Input Characteristics (Common Mode Feedback Amplifier)						
V_{OSC}	Input Offset Voltage	Common Mode, $V_{ID} = 0$		1	± 5 ± 8	mV
	Input Offset Voltage Average Temperature Drift	(Note 10)		25		$\mu V/^{\circ}C$
	Input Bias Current	(Note 9)		-2		μA
	V_{CM} CMRR	$V_{ID} = 0V$, 1V Step on V_{CM} Pin, Measure V_{OD}	70	75		dB
	Input Resistance			25		$k\Omega$
	Common Mode Gain	$\Delta V_{O,CM}/\Delta V_{CM}$	0.995	0.997	1.005	V/V
Output Performance						
	Output Voltage Swing	Peak to Peak, Differential	7.38 7.18	7.8		V
	Output Common Mode Voltage Range	$V_{ID} = 0V$,	± 3.69	± 3.8		V
I_{OUT}	Linear Output Current	$V_{OUT} = 0V$	± 63	± 75		mA
I_{SC}	Short Circuit Current	Output Shorted to Ground $V_{IN} = 3V$ Single Ended (Note 3)		± 200		mA
	Output Balance Error	ΔV_{OUT} Common Mode / ΔV_{OUT} Differential, $V_{OUT} = 1V_{PP}$ Differential, $f = 10$ MHz		-68		dB
Miscellaneous Performance						
	Enable Voltage Threshold	Pin 7	2.0			V
	Disable Voltage Threshold	Pin 7			1.5	V
	Enable Pin Current	$V_{EN} = 0V$ (Note 9)		-250		μA
		$V_{EN} = 4V$ (Note 9)		55		
	Enable/Disable Time			10		ns
A_{VOL}	Open Loop Gain	Differential		70		dB
PSRR	Power Supply Rejection Ratio	DC, $\Delta V_S = \pm 1V$	74	90		dB
	Supply Current	$R_L = \infty$	18	20	24 27	mA
	Disabled Supply Current			1	1.2	mA

5V Electrical Characteristics (Note 2)

Single ended in differential out, $T_A = 25^{\circ}C$, $A_V = +1$, $V_S = 5V$, $V_{CM} = 2.5V$, $R_F = R_G = 365\Omega$, $R_L = 500\Omega$; Unless specified.

Boldface limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
SSBW	Small Signal -3 dB Bandwidth	$R_L = 500\Omega$, $V_{OUT} = 0.5 V_{PP}$		350		MHz
LSBW	Large Signal -3 dB Bandwidth	$R_L = 500\Omega$, $V_{OUT} = 2 V_{PP}$		330		MHz
	0.1 dB Bandwidth			60		MHz
	Slew Rate	2V Step (Note 6)		1500		V/ μs
	Rise/Fall Time, 10% to 90%	1V Step		1		ns
	Settling Time	1V Step, 0.05%		12		ns

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
V_{CM} Pin AC Performance (Common Mode Feedback Amplifier)						
	Common Mode Small Signal Bandwidth			185		MHz
	Slew Rate			180		V/μs
Distortion and Noise Response						
HD2	2 nd Harmonic Distortion	V _O = 2 V _{PP} , f = 5 MHz, R _L = 800Ω		-89		dBc
		V _O = 2 V _{PP} , f = 20 MHz, R _L = 800Ω		-88		
HD3	3 rd Harmonic Distortion	V _O = 2 V _{PP} , f = 5 MHz, R _L = 800Ω		-85		dBc
		V _O = 2 V _{PP} , f = 20 MHz, R _L = 800Ω		-70		
e _n	Input Referred Noise Voltage	f ≥ 1 MHz		6.0		nV/√Hz
i _n	Input Referred Noise Current	f ≥ 1 MHz		1.5		pA/√Hz
Input Characteristics (Differential)						
V _{OSD}	Input Offset Voltage	Differential Mode, V _{ID} = 0, V _{CM} = 0		1	±4 ±6	mV
	Input Offset Voltage Average Temperature Drift	(Note 10)		1.6		μV/°C
I _{BIAS}	Input Bias Current	(Note 9)	0	-8	-16	μA
	Input Bias Current Average Temperature Drift	(Note 10)		9.5		nA/°C
	Input Bias Current Difference	Difference in Bias Currents Between the Two Inputs		0.3		μA
CMRR	Common-Mode Rejection Ratio	DC, V _{ID} = 0V	70	80		dBc
	Input Resistance	Differential		5		MΩ
	Input Capacitance	Differential		1		pF
V _{ICM}	Input Common Mode Range	CMRR > 53 dB	+3.1 +0.4	+3.2 +0.3		
V_{CM} Pin Input Characteristics (Common Mode Feedback Amplifier)						
	Input Offset Voltage	Common Mode, V _{ID} = 0		1	±5 ±8	mV
	Input Offset Voltage Average Temperature Drift			18.6		μV/°C
	Input Bias Current			3		μA
	V _{CM} CMRR	V _{ID} = 0, 1V Step on V _{CM} Pin, Measure V _{OD}	70	75		dB
	Input Resistance	V _{CM} Pin to Ground		25		kΩ
	Common Mode Gain	ΔV _{O,CM} /ΔV _{CM}		0.991		V/V
Output Performance						
V _{OUT}	Output Voltage Swing	Peak to Peak, Differential, V _S = ±2.5V, V _{CM} = 0V	2.4	2.8		V
I _{OUT}	Linear Output Current	V _{OUT} = 0V Differential	±54	±70		mA
I _{SC}	Output Short Circuit Current	Output Shorted to Ground V _{IN} = 3V Single Ended (Note 3)		250		mA
CMVR	Common Mode Voltage Range	V _{ID} = 0, V _{CM} Pin = 1.2V and 3.8V	3.72	3.8		V
			1.23	1.2		
	Output Balance Error	ΔV _{OUT} Common Mode /ΔV _{OUT} Differential, V _{OUT} = 1 V _{PP} Differential, f = 10 MHz		-65		dB

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
Miscellaneous Performance						
	Enable Voltage Threshold	Pin 7	2.0			V
	Disable Voltage Threshold	Pin 7			1.5	V
	Enable Pin Current	$V_{EN} = 0V$ (Note 9)		-250		μA
		$V_{EN} = 4V$ (Note 9)		55		
	Enable/Disable Time			10		ns
	Open Loop Gain	DC, Differential		70		dB
PSRR	Power Supply Rejection Ratio	DC, $\Delta V_S = \pm 0.5V$	72	77		dB
I_S	Supply Current	$R_L = \infty$	16.5	19	23.5 26.5	mA
I_{SD}	Disabled Supply Current			1	1.2	mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

Note 3: The maximum output current (I_{OUT}) is determined by device power dissipation limitations.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for package soldered directly into a 2 layer PC board with zero air flow.

Note 5: Human body model: 1.5 k Ω in series with 100 pF. Machine model: 0 Ω in series with 200pF.

Note 6: Slew Rate is the average of the rising and falling edges.

Note 7: Typical numbers are the most likely parametric norm.

Note 8: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

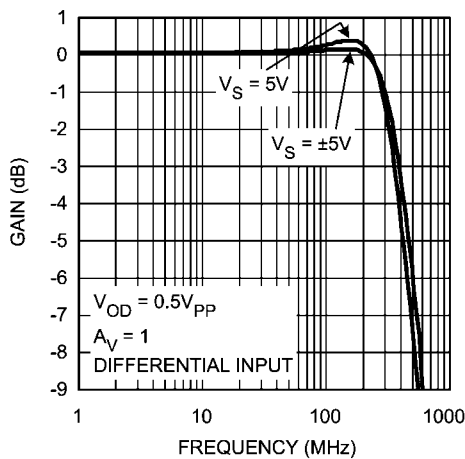
Note 9: Negative input current implies current flowing out of the device.

Note 10: Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

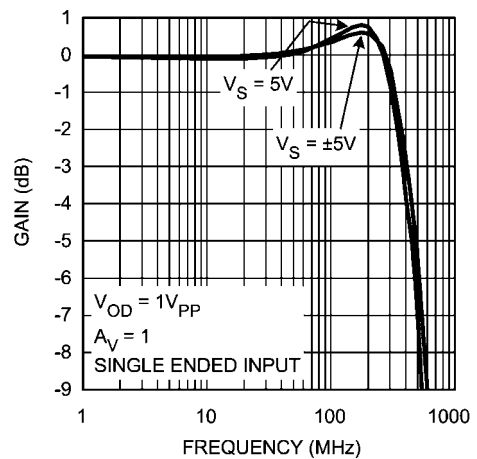
Note 11: Parameter is guaranteed by design.

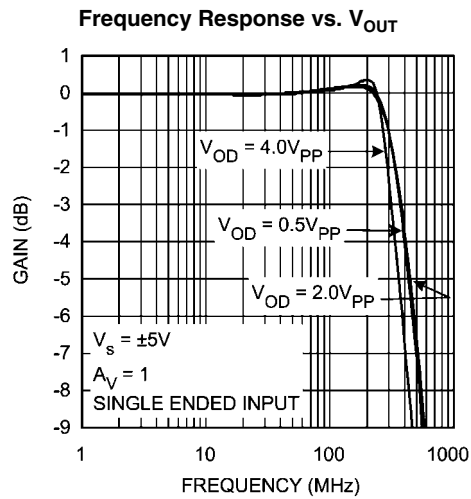
Typical Performance Characteristics ($T_A = 25^\circ C$, $V_S = \pm 5V$, $R_L = 500\Omega$, $R_F = R_G = 365\Omega$; Unless Specified).

Frequency Response vs. Supply Voltage

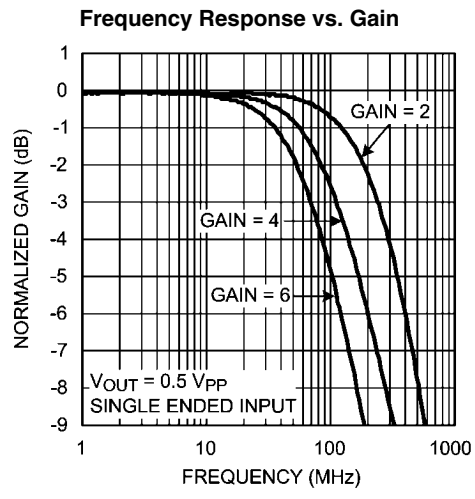


Frequency Response

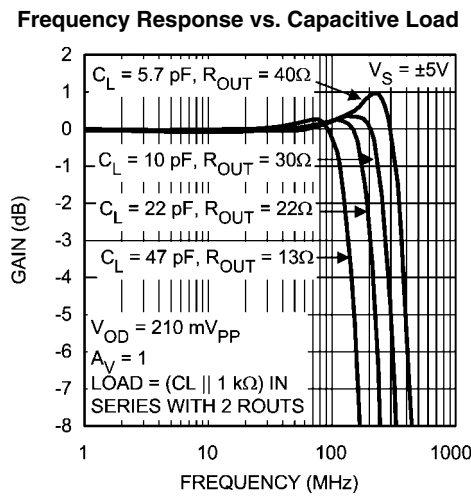




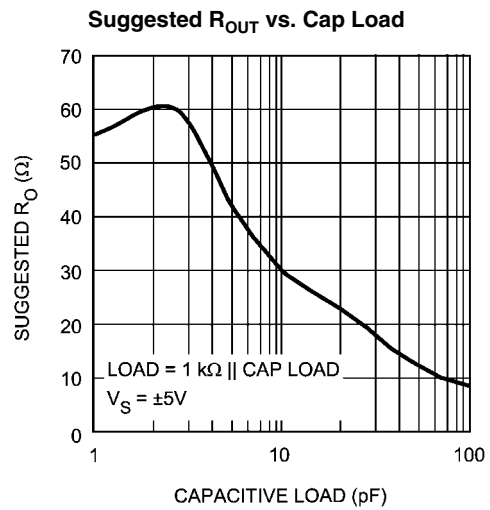
20130116



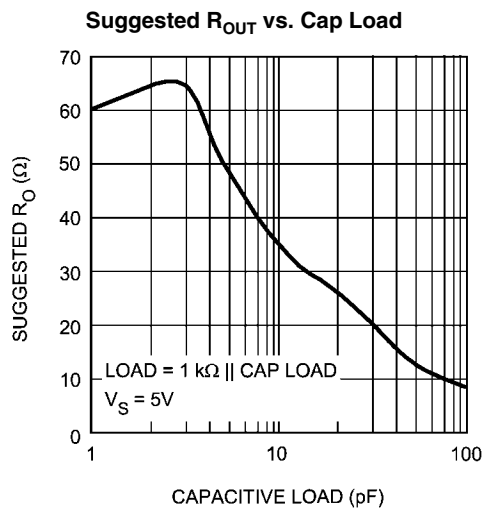
20130134



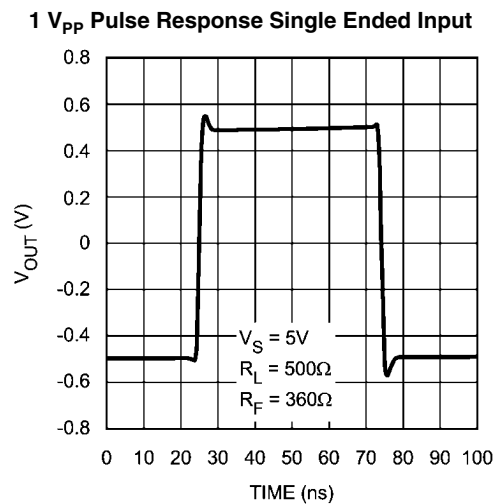
20130121



20130122

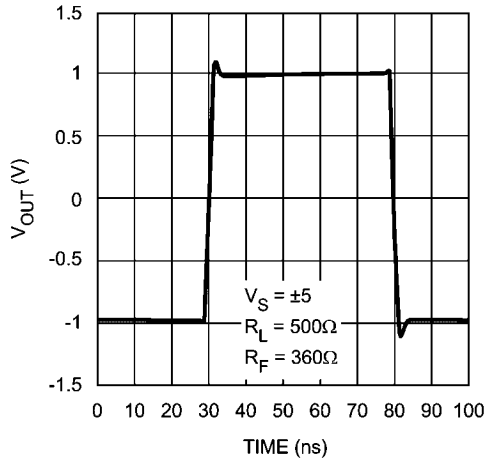


20130123



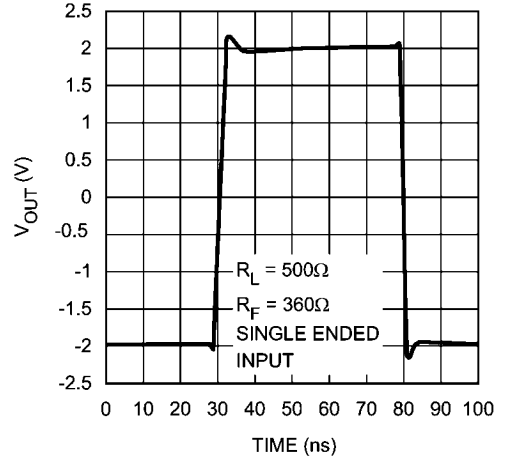
20130126

2 V_{PP} Pulse Response Single Ended Input



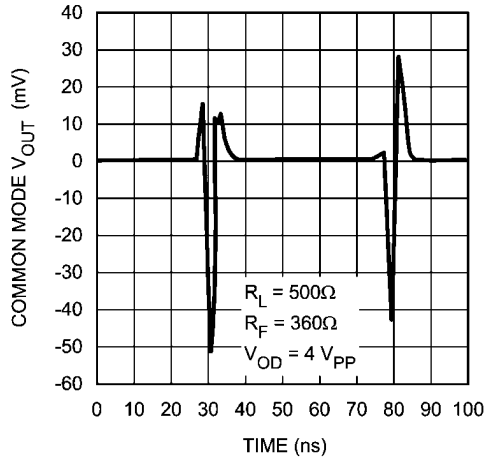
20130127

Large Signal Pulse Response



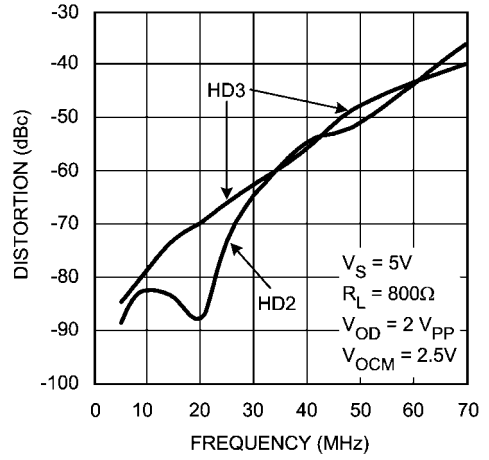
20130125

Output Common Mode Pulse Response



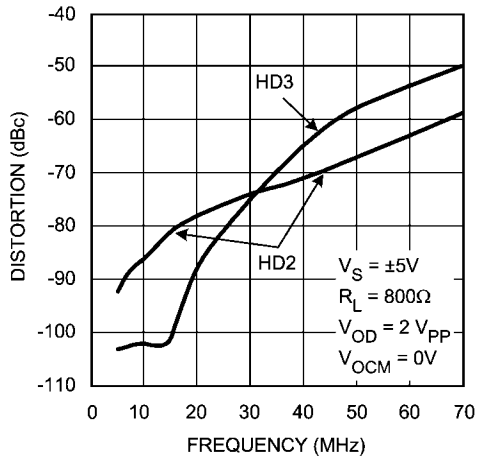
20130124

Distortion vs. Frequency Single Ended Input



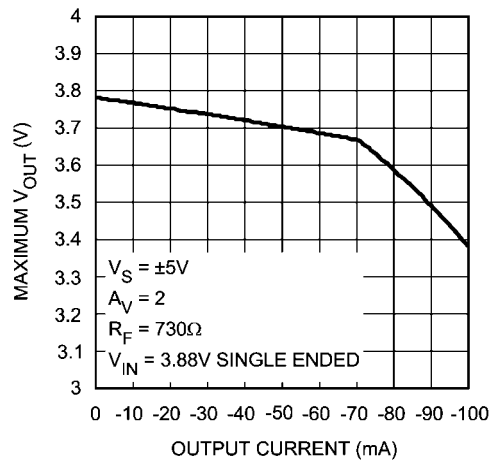
20130128

Distortion vs. Frequency Single Ended Input

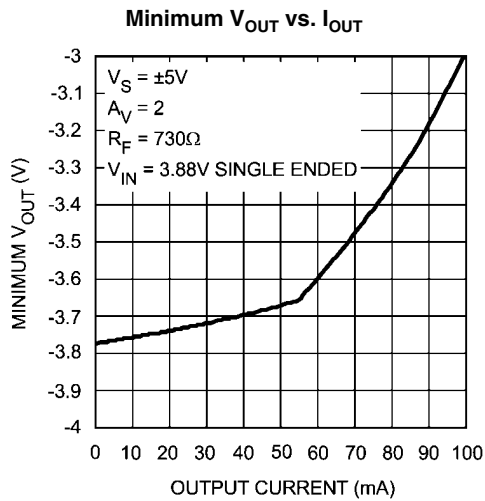


20130129

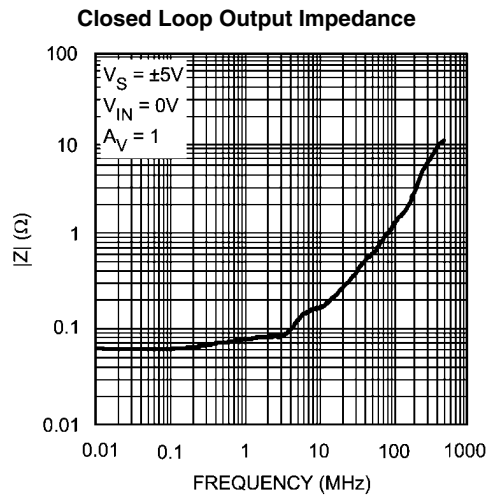
Maximum V_{OUT} vs. I_{OUT}



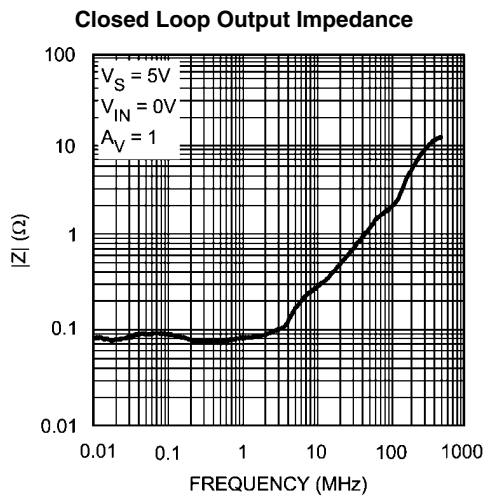
20130130



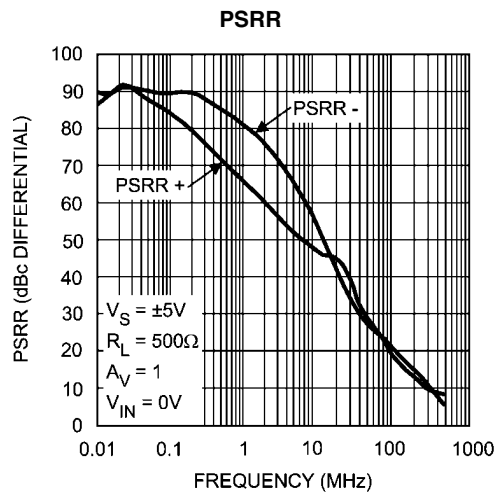
20130131



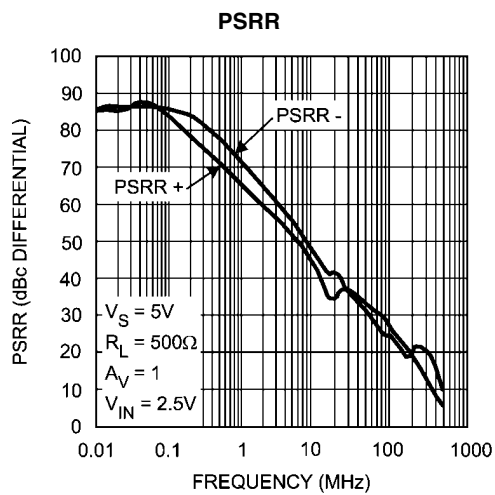
20130117



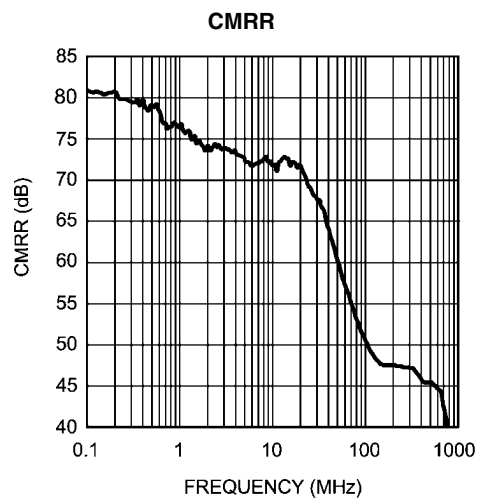
20130118



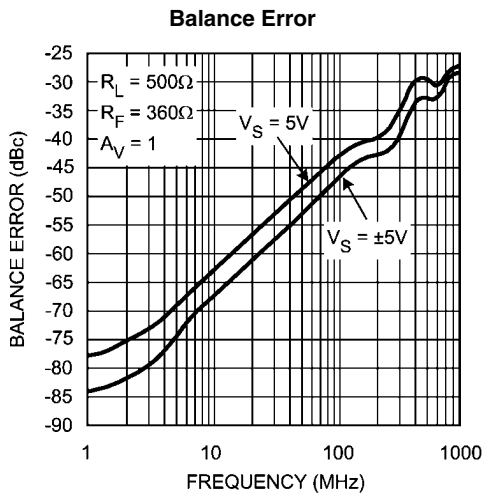
20130119



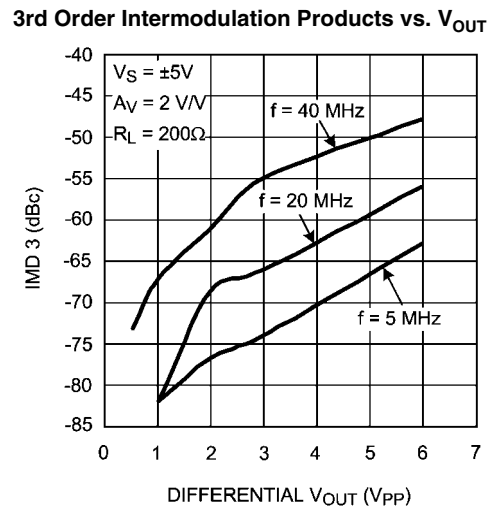
20130120



20130133



20130113



20130135

Application Section

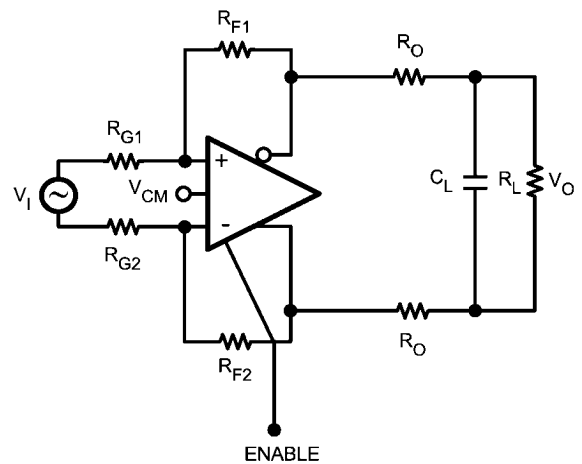
The LMH6550 is a fully differential amplifier designed to provide low distortion amplification to wide bandwidth differential signals. The LMH6550, though fully integrated for ultimate balance and distortion performance, functionally provides three channels. Two of these channels are the V_+ and V_- signal path channels, which function similarly to inverting mode operational amplifiers and are the primary signal paths. The third channel is the common mode feedback circuit. This is the circuit that sets the output common mode as well as driving the V_+ and V_- outputs to be equal magnitude and opposite phase, even when only one of the two input channels is driven. The common mode feedback circuit allows single ended to differential operation.

The LMH6550 is a voltage feedback amplifier with gain set by external resistors. Output common mode voltage is set by the V_{CM} pin. This pin should be driven by a low impedance reference and should be bypassed to ground with a 0.1 μF ceramic capacitor. Any signal coupling into the V_{CM} will be passed along to the output and will reduce the dynamic range of the amplifier.

The LMH6550 is equipped with a ENABLE pin to reduce power consumption when not in use. The ENABLE pin floats to logic high. If this pin is not used it can be left floating. The amplifier output stage goes into a high impedance state when the amplifier is disabled. The feedback and gain set resistors will then set the impedance of the circuit. For this reason input to output isolation will be poor in the disabled state.

FULLY DIFFERENTIAL OPERATION

The LMH6550 will perform best when used with split supplies and in a fully differential configuration. See [Figure 1](#) and [Figure 3](#) for recommend circuits.



20130104

FIGURE 1. Typical Application

The circuit shown in [Figure 1](#) is a typical fully differential application as might be used to drive an ADC. In this circuit closed loop gain, $(A_V) = V_{OUT}/V_{IN} = R_F/R_G$. For all the applications in this data sheet V_{IN} is presumed to be the voltage presented to the circuit by the signal source. For differential signals this will be the difference of the signals on each input (which will be double the magnitude of each individual signal), while in single ended inputs it will just be the driven input signal.

The resistors R_O help keep the amplifier stable when presented with a load C_L as is typical in an analog to digital converter (ADC). When fed with a differential signal, the LMH6550 provides excellent distortion, balance and common mode rejection provided the resistors R_F , R_G and R_O are well matched and strict symmetry is observed in board layout. With a DC CMRR of over 80 dB, the DC and low frequency CMRR of most circuits will be dominated by the external resistors and board trace resistance. At higher frequencies board layout symmetry becomes a factor as well. Precision resistors of at least 0.1% accuracy are recommended and careful board layout will also be required.

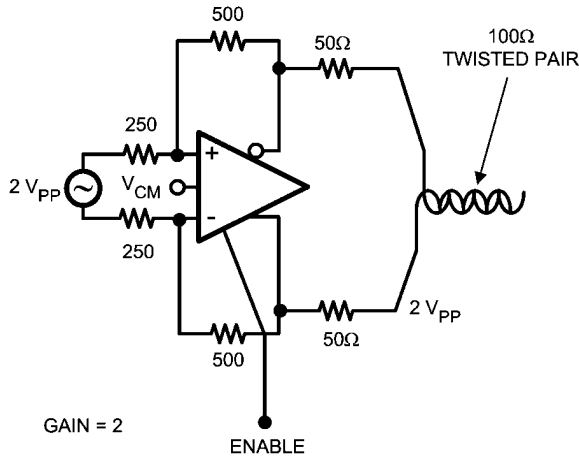
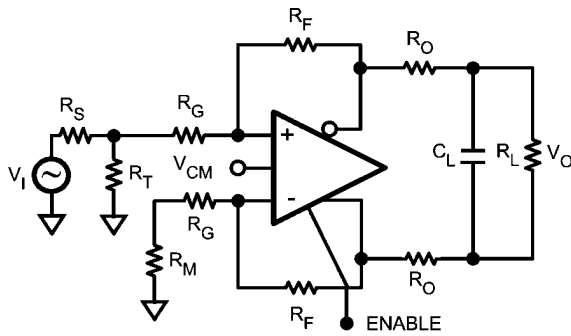


FIGURE 2. Fully Differential Cable Driver

With up to 15 V_{pp} differential output voltage swing and 80 mA of linear drive current the LMH6550 makes an excellent cable driver as shown in *Figure 2*. The LMH6550 is also suitable for driving differential cables from a single ended source.



$$\text{SET } R_M = R_T || R_S$$

$$\text{SET } R_T = \frac{1}{\left(\frac{1}{R_S} - \frac{1}{R_{IN}}\right)} \quad R_{IN} = \frac{R_G}{1 - \left(\frac{R_F}{2 * (R_F + R_G)}\right)}$$

FIGURE 3. Single Ended in Differential Out

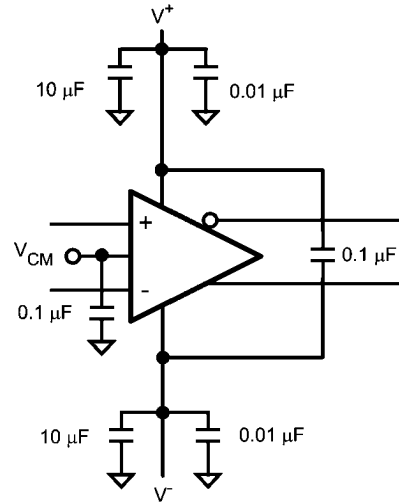


FIGURE 4. Split Supply Bypassing Capacitors

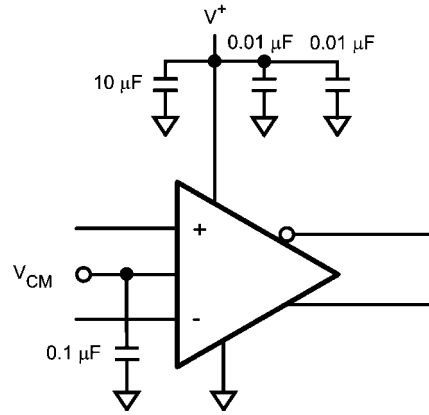


FIGURE 5. Single Supply Bypassing Capacitors

The LMH6550 requires supply bypassing capacitors as shown in *Figure 4* and *Figure 5*. The 0.01 μF and 0.1 μF capacitors should be leadless SMT ceramic capacitors and should be no more than 3 mm from the supply pins. The SMT capacitors should be connected directly to a ground plane. Thin traces or small vias will reduce the effectiveness of bypass capacitors. Also shown in both figures is a capacitor from the V_{CM} pin to ground. The V_{CM} pin is a high impedance input to a buffer which sets the output common mode voltage. Any noise on this input is transferred directly to the output. Output common mode noise will result in loss of dynamic range, degraded CMRR, degraded Balance and higher distortion. The V_{CM} pin should be bypassed even if the pin is not used. There is an internal resistive divider on chip to set the output common mode voltage to the mid point of the supply pins. The impedance looking into this pin is approximately 25 kΩ. If a different output common mode voltage is desired drive this pin with a clean, accurate voltage reference.

SINGLE ENDED INPUT TO DIFFERENTIAL OUTPUT

The LMH6550 provides excellent performance as an active balun transformer. *Figure 3* shows a typical application where an LMH6550 is used to produce a differential signal from a single ended source.

In single ended input operation the output common mode voltage is set by the V_{CM} pin as in fully differential mode. Also, In this mode the common mode feedback circuit must recreate the signal that is not present on the unused differential input pin. The performance chart titled “Balance Error” is the measurement of the effectiveness of this process. The common mode feedback circuit is responsible for ensuring balanced output with a single ended input. Balance error is defined as the amount of input signal that couples into the output common mode. It is measured as a the undesired output common mode swing divided by the signal on the input. Balance error can be caused by either a channel to channel gain error, or phase error. Either condition will produce a common mode shift. The chart titled “Balance Error” measures the balance error with a single ended input as that is the most demanding mode of operation for the amplifier.

Supply and V_{CM} pin bypassing are also critical in this mode of operation. See the above section on FULLY DIFFERENTIAL

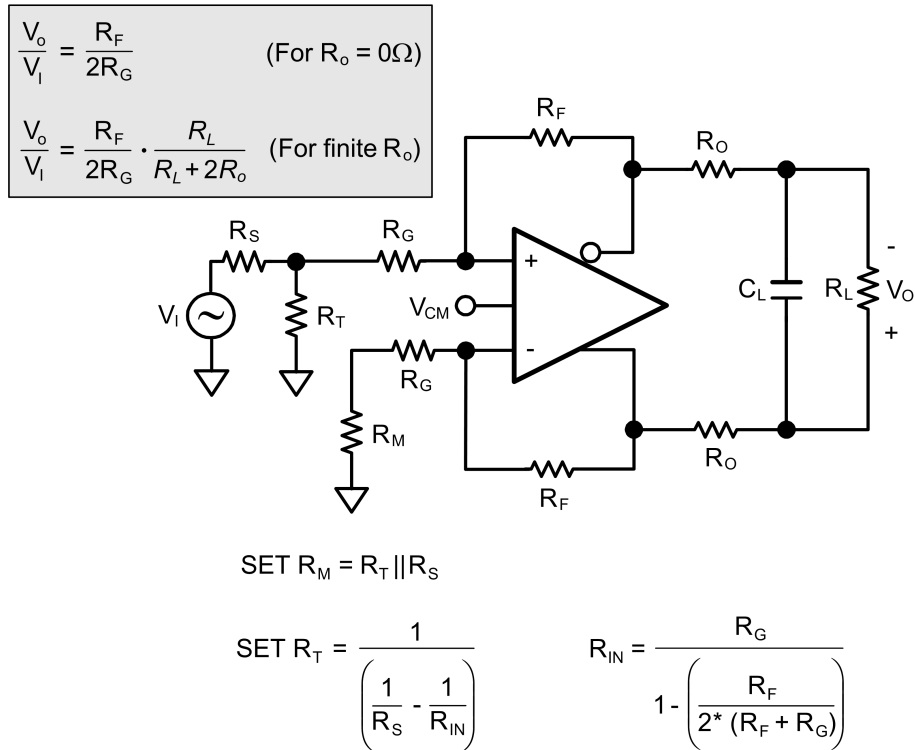
OPERATION for bypassing recommendations also see *Figure 4* and *Figure 5* for recommended supply bypassing configurations.

SINGLE SUPPLY OPERATION

The input stage of the LMH6550 has a built in offset of 0.7V towards the lower supply to accommodate single supply operation with single ended inputs. As shown in *Figure 6*, the input common mode voltage is less than the output common mode voltage. It is set by current flowing through the feedback network from the device output. The input common mode range of 0.4V to 3.2V places constraints on gain settings. Possible solutions to this limitation include AC coupling the input signal, using split power supplies and limiting stage gain. AC coupling with single supply is shown in *Figure 7*.

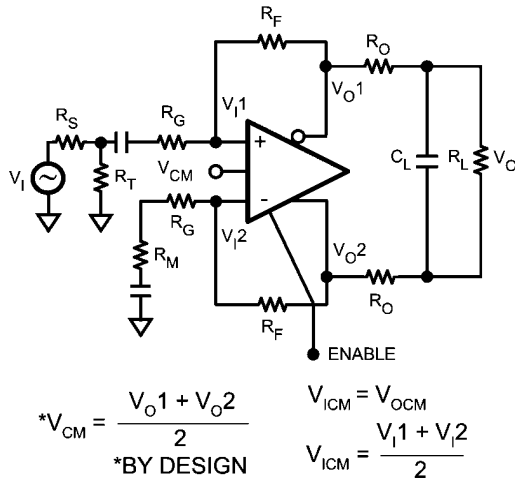
In *Figure 6* closed loop gain = $V_O / V_I = R_F / 2R_G$. Note that in single ended to differential operation V_I is measured single ended while V_O is measured differentially. This means that gain is really 1/2 or 6 dB less when measured on either of the output pins separately. Additionally, note that the input signal at R_T is 1/2 of V_I when R_T is chosen to match R_S to R_{IN} .

$V_{ICM} = \text{Input common mode voltage} = (V_{+IN} + V_{-IN}) / 2.$



20130136

FIGURE 6. Relating Gain to Input / Output Common Mode Voltages

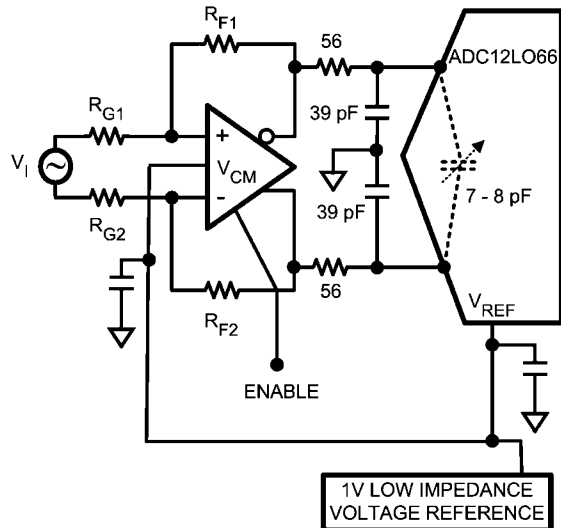


20130109

FIGURE 7. AC Coupled for Single Supply Operation

DRIVING ANALOG TO DIGITAL CONVERTERS

Analog to digital converters (ADC) present challenging load conditions. They typically have high impedance inputs with large and often variable capacitive components. As well, there are usually current spikes associated with switched capacitor or sample and hold circuits. *Figure 8* shows a typical circuit for driving an ADC. The two 56Ω resistors serve to isolate the capacitive loading of the ADC from the amplifier and ensure stability. In addition, the resistors form part of a low pass filter which helps to provide anti alias and noise reduction functions. The two 39 pF capacitors help to smooth the current spikes associated with the internal switching circuits of the ADC and also are a key component in the low pass filtering of the ADC input. In the circuit of *Figure 8* the cutoff frequency of the filter is $1 / (2 * \pi * 56\Omega * (39 \text{ pF} + 14 \text{ pF})) = 53 \text{ MHz}$ (which is slightly less than the sampling frequency). Note that the ADC input capacitance must be factored into the frequency response of the input filter, and that being a differential input the effective input capacitance is double. Also as shown in *Figure 8* the input capacitance to many ADCs is variable based on the clock cycle. See the data sheet for your particular ADC for details.



20130105

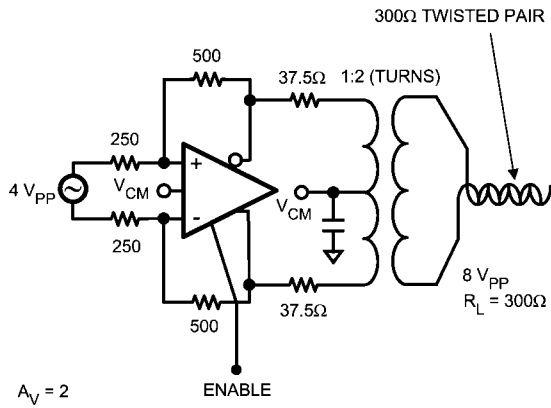
FIGURE 8. Driving an ADC

The amplifier and ADC should be located as closely together as possible. Both devices require that the filter components be in close proximity to them. The amplifier needs to have minimal parasitic loading on the output traces and the ADC is sensitive to high frequency noise that may couple in on its input lines. Some high performance ADCs have an input stage that has a bandwidth of several times its sample rate. The sampling process results in all input signals presented to the input stage mixing down into the Nyquist range (DC to $F_s/2$). See AN-236 for more details on the subsampling process and the requirements this imposes on the filtering necessary in your system.

USING TRANSFORMERS

Transformers are useful for impedance transformation as well as for single to differential, and differential to single ended conversion. A transformer can be used to step up the output voltage of the amplifier to drive very high impedance loads as shown in *Figure 9*. *Figure 11* shows the opposite case where the output voltage is stepped down to drive a low impedance load.

Transformers have limitations that must be considered before choosing to use one. Compared to a differential amplifier, the most serious limitations of a transformer are the inability to pass DC and balance error (which causes distortion and gain errors). For most applications the LMH6550 will have adequate output swing and drive current and a transformer will not be desirable. Transformers are used primarily to interface differential circuits to 50Ω single ended test equipment to simplify diagnostic testing.



$A_V = 2$

20130107

FIGURE 9. Transformer Out High Impedance Load

$$V_L = \frac{V_{IN} * A_V * N}{\left(\frac{2 R_{OUT} * N^2}{R_L} + 1 \right)}$$

WHERE V_{IN} = DIFFERENTIAL INPUT VOLTAGE

N = TRANSFORMER TURNS RATIO = $\left(\frac{\text{SECONDARY}}{\text{PRIMARY}} \right)$

A_V = CLOSED LOOP AMPLIFIER GAIN

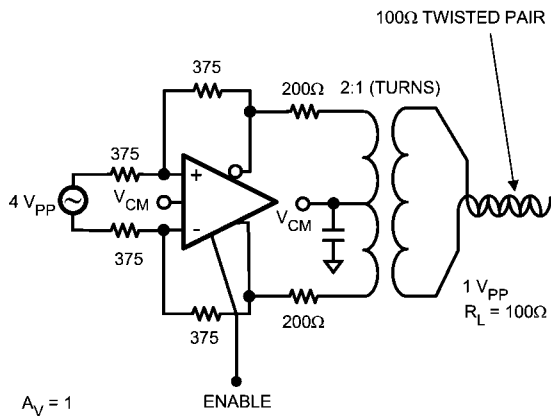
R_{OUT} = SERIES OUTPUT MATCHING RESISTOR

R_L = LOAD RESISTOR

V_L = VOLTAGE ACROSS LOAD RESISTOR

20130132

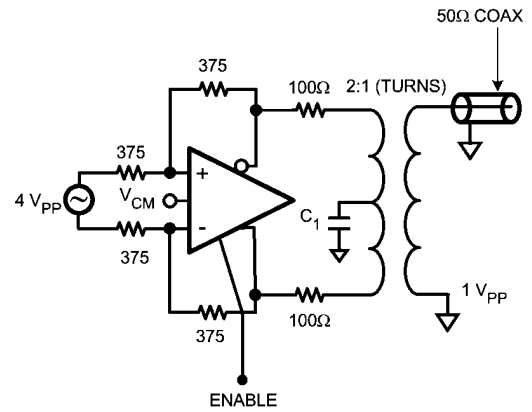
FIGURE 10. Calculating Transformer Circuit Net Gain



$A_V = 1$

20130106

FIGURE 11. Transformer Out Low Impedance Load



GAIN = 1

C_1 IS NOT REQUIRED IF V_{CM} = GROUND

20130103

FIGURE 12. Driving 50Ω Test Equipment

CAPACITIVE DRIVE

As noted in the Driving ADC section, capacitive loads should be isolated from the amplifier output with small valued resistors. This is particularly the case when the load has a resistive component that is 500Ω or higher. A typical ADC has capacitive components of around 10 pF and the resistive component could be 1000Ω or higher. If driving a transmission line, such as 50Ω coaxial or 100Ω twisted pair, using matching resistors will be sufficient to isolate any subsequent capacitance. For other applications see the “Suggested R_{OUT} vs. Cap Load” charts in the Typical Performance Characteristics section.

POWER DISSIPATION

The LMH6550 is optimized for maximum speed and performance in the small form factor of the standard SOIC package, and is essentially a dual channel amplifier. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} of 150°C is never exceeded due to the overall power dissipation.

Follow these steps to determine the Maximum power dissipation for the LMH6550:

1. Calculate the quiescent (no-load) power: $P_{AMP} = I_{CC} * (V_S)$, where $V_S = V+ - V-$. (Be sure to include any current through the feedback network if V_{OCM} is not mid rail.)
2. Calculate the RMS power dissipated in each of the output stages: P_D (rms) = rms $((V_S - V_{OUT}^+) * I_{OUT}^+) +$ rms $((V_S - V_{OUT}^-) * I_{OUT}^-)$, where V_{OUT} and I_{OUT} are the voltage and the current measured at the output pins of the differential amplifier as if they were single ended amplifiers and V_S is the total supply voltage.
3. Calculate the total RMS power: $P_T = P_{AMP} + P_D$.

The maximum power that the LMH6550 package can dissipate at a given temperature can be derived with the following equation:

$P_{MAX} = (150 - T_{AMB}) / \theta_{JA}$, where T_{AMB} = Ambient temperature (°C) and θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W). For the SOIC package θ_{JA} is 150° C/W, and for the MSOP package it is 235° C/W.

NOTE: If V_{CM} is not 0V then there will be quiescent current flowing in the feedback network. This current should be in-

cluded in the thermal calculations and added into the quiescent power dissipation of the amplifier.

ESD PROTECTION

The LMH6550 is protected against electrostatic discharge (ESD) on all pins. The LMH6550 will survive 2000V Human Body model and 200V Machine model events. Under normal operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6550 is driven by a large signal while the device is powered down the ESD diodes will conduct. The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Using the shutdown mode is one way to conserve power and still prevent unexpected operation.

BOARD LAYOUT

The LMH6550 is a very high performance amplifier. In order to get maximum benefit from the differential circuit architecture board layout and component selection is very critical. The circuit board should have low inductance ground plane and well bypassed broad supply lines. External components

should be leadless surface mount types. The feedback network and output matching resistors should be composed of short traces and precision resistors (0.1%). The output matching resistors should be placed within 3-4 mm of the amplifier as should the supply bypass capacitors. The LMH730154 evaluation board is an example of good layout techniques.

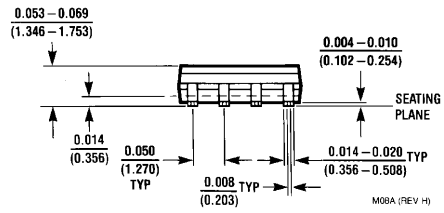
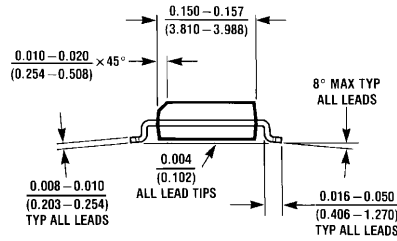
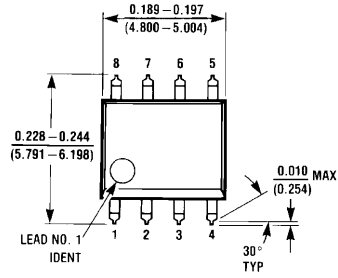
The LMH6550 is sensitive to parasitic capacitances on the amplifier inputs and to a lesser extent on the outputs as well. Ground and power plane metal should be removed from beneath the amplifier and from beneath R_F and R_G .

With any differential signal path symmetry is very important. Even small amounts of asymmetry will contribute to distortion and balance errors.

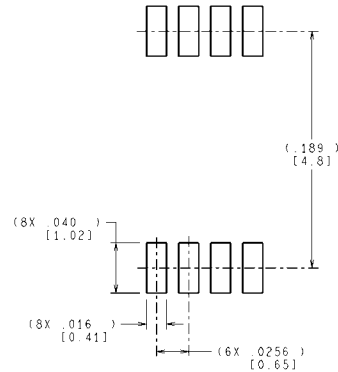
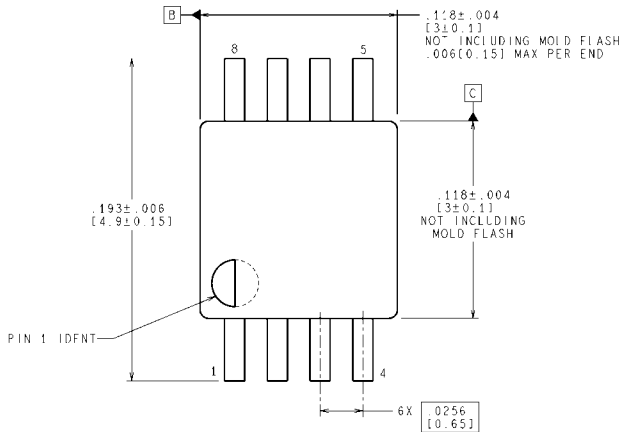
EVALUATION BOARD

National Semiconductor offers evaluation board(s) to aid in device testing and characterization and as a guide for proper layout. Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information).

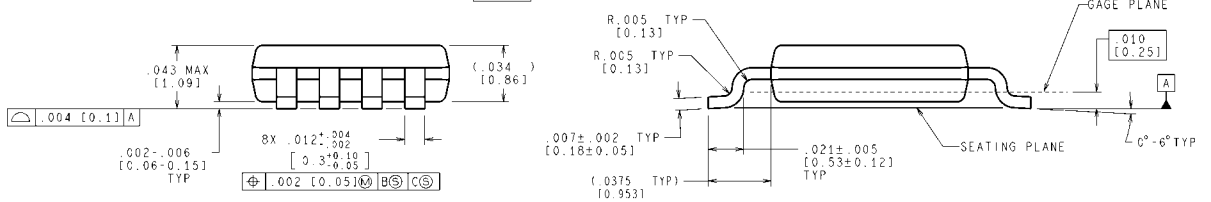
Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin SOIC
NS Package Number M08A



RECOMMENDED LAND PATTERN



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

8-Pin MSOP
NS Package Number MUA08A

MUA08A (Rev F)

Notes

LMH6550

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:
www.national.com

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempensors	SolarMagic™	www.national.com/solarmagic
PLL/VCO	www.national.com/wireless	PowerWise® Design University	www.national.com/training

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2011 National Semiconductor Corporation

For the most current product information visit us at www.national.com



National Semiconductor
Americas Technical
Support Center
Email: support@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe
Technical Support Center
Email: europe.support@nsc.com

National Semiconductor Asia
Pacific Technical Support Center
Email: ap.support@nsc.com

National Semiconductor Japan
Technical Support Center
Email: jpn.feedback@nsc.com