IXYS IXDN430 / IXDI430 / IXDD430 / IXDS430

30 Amp Low-Side Ultrafast MOSFET / IGBT Driver

Features

- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up Protected
- High Peak Output Current: 30A Peak
- Wide Operating Range: 8.5V to 35V
- Under Voltage Lockout Protection
- Ability to Disable Output under Faults
- High Capacitive Load Drive Capability: 5600 pF in <25ns
- Matched Rise And Fall Times
- Low Propagation Delay Time
- Low Output Impedance
- Low Supply Current

Applications

- Driving MOSFETs and IGBTs
- Motor Controls
- Line Drivers
- Pulse Generators
- Local Power ON / OFF Switch
- Switch Mode Power Supplies (SMPS)
- DC to DC Converters
- Pulse Transformer Driver
- Limiting di/dt Under Short Circuit
- Class D Switching Amplifiers

General Description

The IXDN430/IXDI430/IXDD430/IXDS430 are high speed high current gate drivers specifically designed to drive MOSFETs and IGBTs to their minimum switching time and maximum practical frequency limits. The IXD_430 can source and sink 30A of peak current while producing voltage rise and fall times of less than 30ns. The input of the drivers are compatible with TTL or CMOS and are fully immune to latch up over the entire operating range. Designed with small internal delays, cross conduction/current shoot-through is virtually eliminated in all configurations. Their features and wide safety margin in operating voltage and power make the drivers unmatched in performance and value.

The IXD_430 incorporates a unique ability to disable the output under fault conditions. The standard undervoltage lockout is at 12.5V which can also be set to 8.5V in the IXDS430SI. When a logical low is forced into the Enable inputs, both final output stage MOSFETs (NMOS and PMOS) are turned off. As a result, the output of the IXDD430 enters a tristate mode and enables a Soft Turn-Off of the MOSFET when a short circuit is detected. This helps prevent damage that could occur to the MOSFET if it were to be switched off abruptly due to a dv/dt over-voltage transient.

The IXDN430 is configured as a noninverting gate driver, and the IXDI430 is an inverting gate driver. The IXDS430 can be configured either as a noninverting or inverting driver. The IXD_430 are available in the standard 28-pin SIOC (SI-CT), 5-pin TO-220 (CI), and in the TO-263 (YI) surface mount packages. CT or 'Cool Tab' for the 28-pin SOIC package refers to the backside metal heatsink tab.

Ordering Information

Part Number	Package Type	Temp. Range	Configuration
IXDD430YI	5-pin TO-263	-55°C to +125°	Non Inverting with Enable
IXDD430CI	5-pin TO-220		
IXDI430YI	5-pin TO-263	-55°C to +125°	Inverting
IXDI430CI	5-pin TO-220		
IXDN430YI	5-pin TO-263	-55°C to +125°	Non Inverting
IXDN430CI	5-pin TO-220		
IXDS430SI	28-pin SOIC	-55°C to +125°	Inverting / Non Inverting with Enable and UVSEL

Figure 1A - IXDD430 (Non Inverting With Enable) Diagram

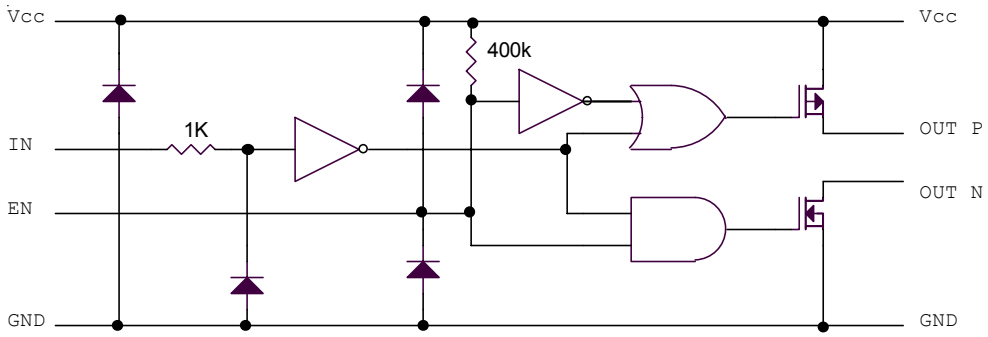


Figure 1B - IXDN430 (Non-Inverting) Diagram

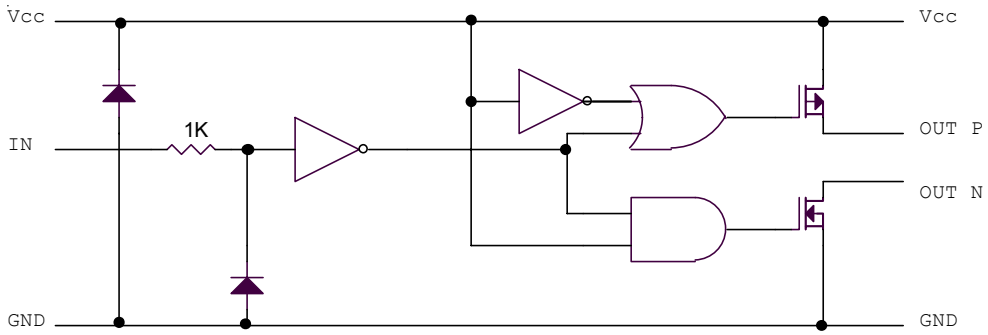


Figure 1C - IXDI430 (Inverting) Diagram

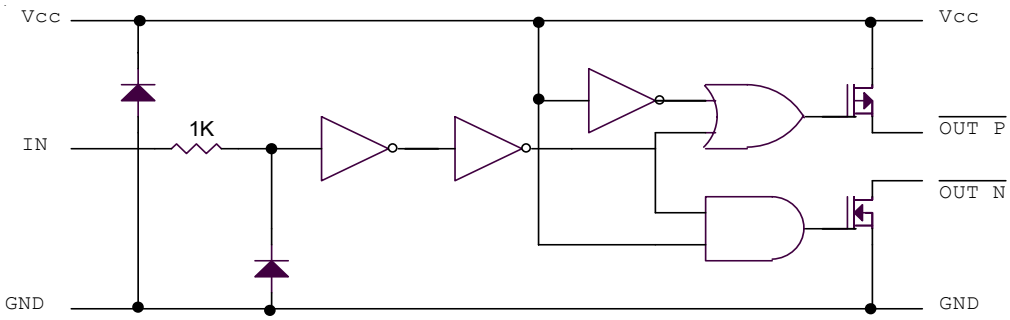
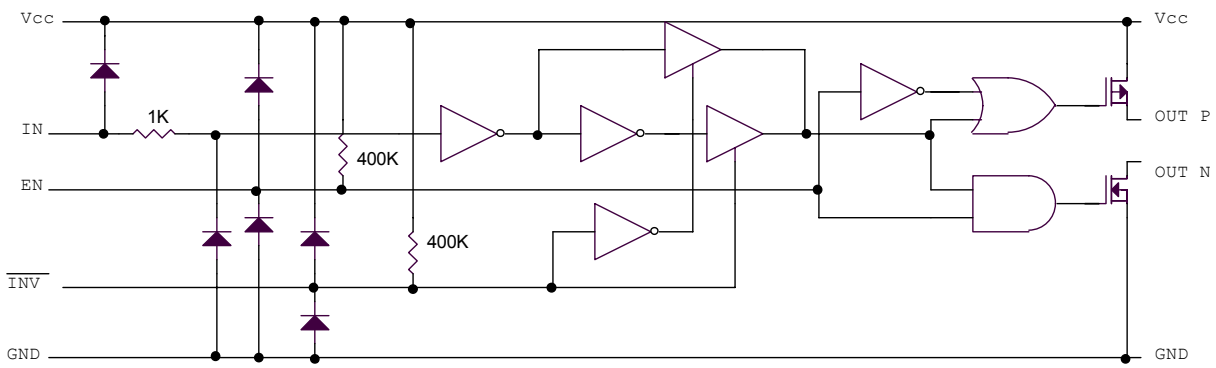


Figure 1D - IXDS430 (Inverting and Non Inverting with Enable) Diagram



Note: Out P and Out N are connected together in the 5 lead TO-220 and TO-263 packages.

Absolute Maximum Ratings (Note 1)

Parameter	Value
Supply Voltage	40 V
All Other Pins	-0.3 V to V_{CC} + 0.3 V
Power Dissipation, $T_{AMBIENT}$ ≤25 °C TO220 (CI), TO263 (YI)	2W
Derating Factors (to Ambient) TO220 (CI), TO263 (YI)	0.016W/°C
Storage Temperature	-65 °C to 150 °C
Lead Temperature (10 sec)	300 °C

Operating Ratings

Parameter	Value
Maximum Junction Temperature	150 °C
Operating Temperature Range	-55 °C to 125 °C
Thermal Impedance TO220 (CI), TO263 (YI)	
θ_{JC} (Junction To Case)	0.95 °C/W
θ_{JA} (Junction To Ambient)	62.5 °C/W
Thermal Impedance 28 pin SOIC with Heat Slug (SI)	
θ_{JC} (Junction To Case)	3 °C/W

Electrical Characteristics

Unless otherwise noted, T_A = 25 °C, 8.5V ≤ V_{CC} ≤ 35V .
All voltage measurements with respect to GND. IXDD430 configured as described in *Test Conditions*.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	High input voltage	4.5V ≤ V_{CC} ≤ 18V	3.5			V
V_{IL}	Low input voltage	4.5V ≤ V_{CC} ≤ 18V			0.8	V
V_{IN}	Input voltage range		-5		V_{CC} + 0.3	V
I_{IN}	Input current	0V ≤ V_{IN} ≤ V_{CC}	-10		10	µA
V_{OH}	High output voltage		V_{CC} - 0.025			V
V_{OL}	Low output voltage				0.025	V
R_{OH}	Output resistance @ Output high	V_{CC} = 18V		0.3	0.4	Ω
R_{OL}	Output resistance @ Output Low	V_{CC} = 18V		0.2	0.3	Ω
I_{PEAK}	Peak output current	V_{CC} = 18V		30		A
I_{DC}	Continuous output current	Limited by package power dissipation			8	A
V_{EN}	Enable voltage range	IXDD430 Only	- 0.3		Vcc + 0.3	V
V_{ENH}	High En Input Voltage	IXDD430 Only	2/3 Vcc			V
V_{ENL}	Low En Input Voltage	IXDD430 Only			1/3 Vcc	V
R_{EN}	EN Input Resistance	IXDS430 Only		400		Kohm
V_{INV}	INV Voltage Range	IXDS430 Only	- 0.3		Vcc + 0.3	V
V_{INVH}	High INV Input Voltage	IXDS430 Only	2/3 Vcc			V
V_{INVL}	Low INV Input Voltage	IXDS430 Only			1/3 Vcc	V
R_{INV}	INV Input Resistance	IXDS430 Only		400		Kohm
t_R	Rise time	C_L=5600pF Vcc=18V		18	20	ns
t_F	Fall time	C_L=5600pF Vcc=18V		16	18	ns
t_{ONDLY}	On-time propagation delay	C_L=5600pF Vcc=18V		41	45	ns
t_{OFFDLY}	Off-time propagation delay	C_L=5600pF Vcc=18V		35	39	ns
t_{ENOH}	Enable to output high delay time	IXDD430 Only, Vcc=18V			47	ns
t_{DOLD}	Disable to output low delay time	IXDD430 Only, Vcc=18V			120	ns
V_{CC}	Power supply voltage		8.5	18	35	V
I_{CC}	Power supply current	V_{IN} = 3.5V V_{IN} = 0V V_{IN} = + V_{CC}		1 0	3 10 10	mA µA µA

Specifications Subject To Change Without Notice

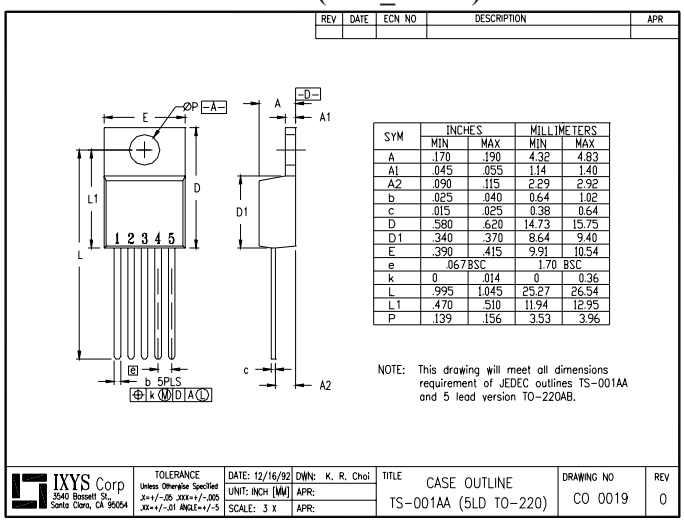
Note 1: Operating the device beyond parameters with listed "absolute maximum ratings" may cause permanent damage to the device. Typical values indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. The guaranteed specifications apply only for the test conditions listed. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Electrical Characteristics

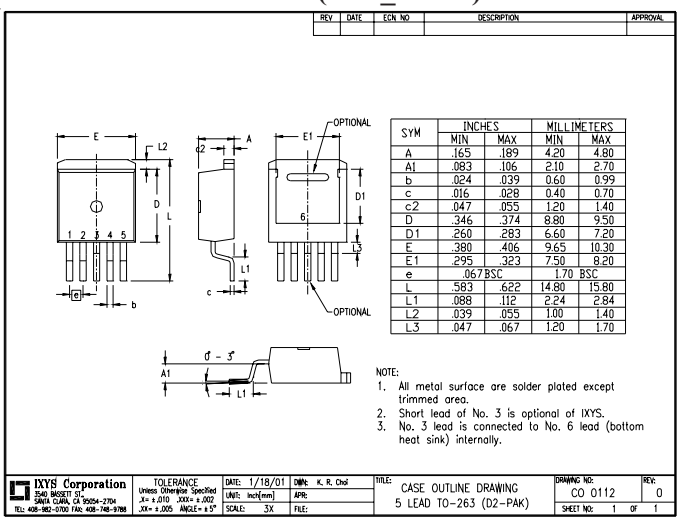
Unless otherwise noted, temperature over -55 °C to +125 °C, $4.5 \le V_{CC} \le 35V$.
All voltage measurements with respect to GND. IXDD430 configured as described in *Test Conditions*.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	High input voltage	$4.5V \le V_{CC} \le 18V$	3.2			V
V_{IL}	Low input voltage	$4.5V \le V_{CC} \le 18V$			1.1	V
V_{IN}	Input voltage range		-5		V_{CC} + 0.3	V
R_{OH}	Output resistance @ Output high	V_{CC} = 18V			0.46	Ω
R_{OL}	Output resistance @ Output Low	V_{CC} = 18V			0.4	Ω
t_R	Rise time	C_L=5600pF Vcc=18V			20	ns
t_F	Fall time	C_L=5600pF Vcc=18V			18	ns
t_{ONDLY}	On-time propagation delay	C_L=5600pF Vcc=18V			58	ns
t_{OFFDLY}	Off-time propagation delay	C_L=5600pF Vcc=18V			51	ns
V_{CC}	Power supply voltage		8.5	18	35	V

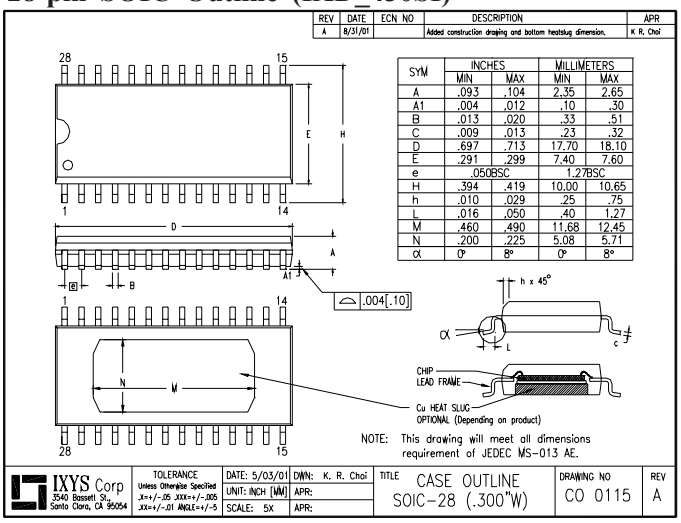
5-lead TO-220 Outline (IXD_430CI)



5-lead TO-263 Outline (IXD_430YI)

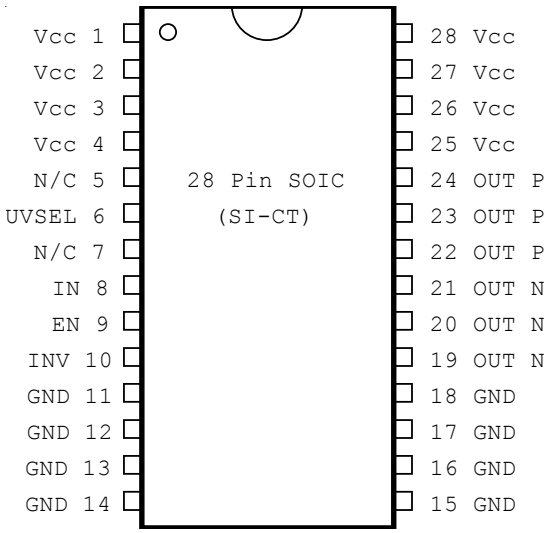


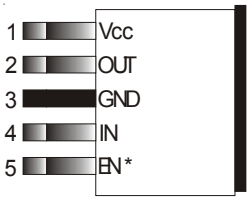
28-pin SOIC Outline (IXD_430SI)



NOTE: Mounting tabs, solder tabs, or heat sink metalization on all packages are connected to ground.

Pin Configurations





TO220 (CI)
TO263 (YI)

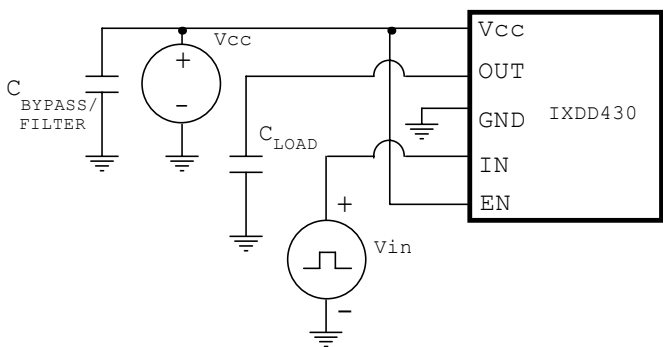
Pin Description

SYMBOL	FUNCTION	DESCRIPTION
VCC	Supply Voltage	Positive power-supply voltage input. This pin provides power to the entire chip. The range for this voltage is from 8.5V to 35V.
IN	Input	Input signal-TTL or CMOS compatible.
EN *	Enable	The system enable pin. This pin, when driven low, disables the chip, forcing high impedance state to the output (IXDD430 Only).
INV	Invert	Forcing INV low causes the IXDS430 to become non-inverted, while forcing INV high causes the IXDS430 to become inverted.
OUT P OUT N	Output	Respective P and N driver outputs. For application purposes this pin is connected, through a resistor, to Gate of a MOSFET/IGBT. The P and N output pins are connected together in the TO-263 and TO-220 packages.
GND	Ground	The system ground pin. Internally connected to all circuitry, this pin provides ground reference for the entire chip. This pin should be connected to a low noise analog ground plane for optimum performance.
UVSEL	Select Under Voltage Level	With UVSEL connected to Vcc, IXDS430 outputs go low at Vcc < 8.5V; With UVSEL open, under voltage level is set at Vcc < 12.5V

* This pin is used only on the IXDD430, and is N/C (not connected) on the IXDI430 and IXDN430.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD procedures when handling and assembling this component.

Figure 2 - Characteristics Test Diagram



Typical Performance Characteristics

Fig. 3 Rise Times vs. Supply Voltage

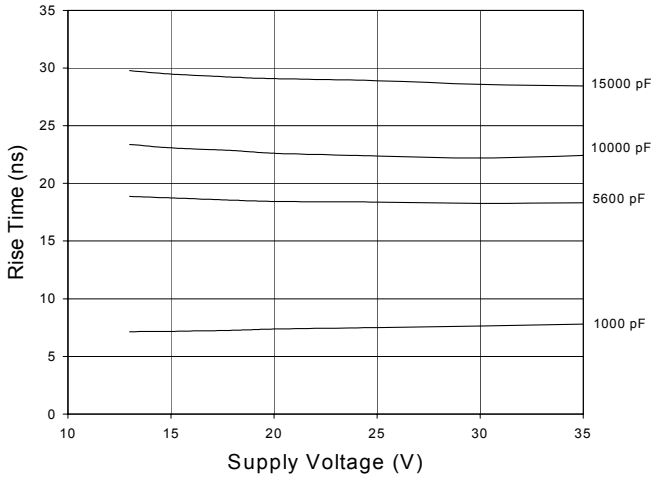


Fig. 4 Fall Times vs. Supply Voltage

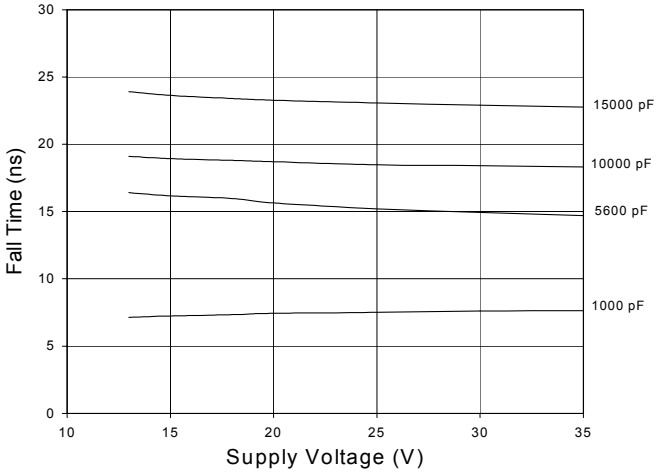


Fig. 5 Output Rise Times vs. Load Capacitance

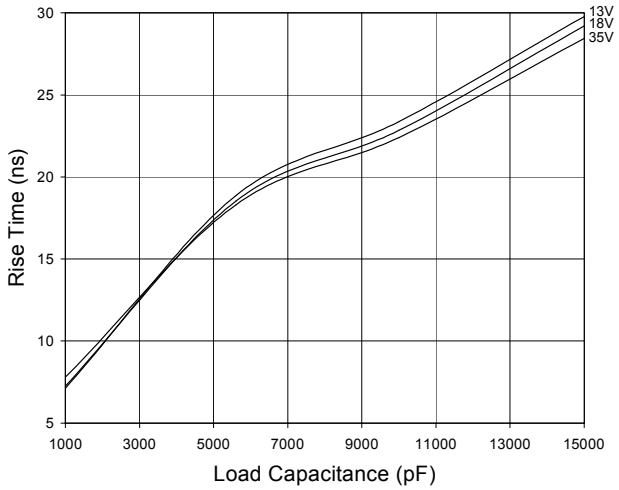


Fig. 6 Output Fall Times vs. Load Capacitance

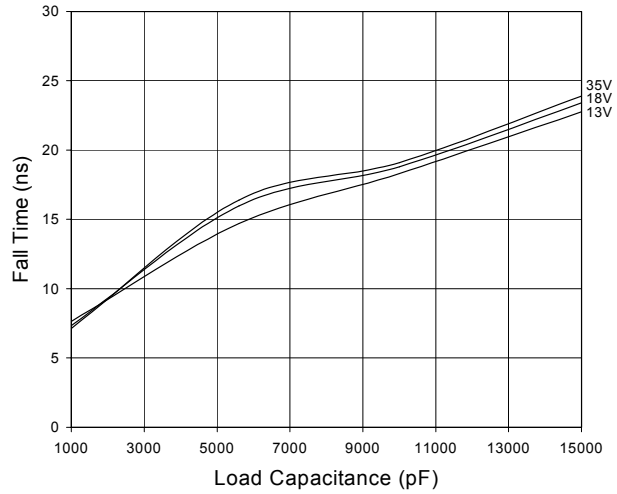


Fig. 7 Rise and Fall Times vs. Temperature
C_L = 5600 pF, Vcc = 18V

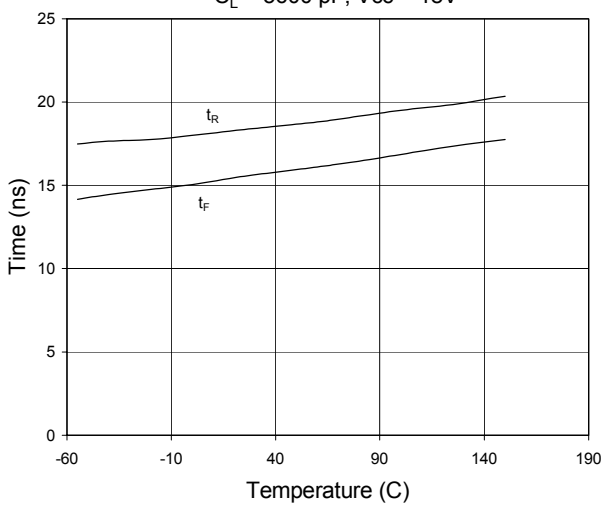


Fig. 8 Max / Min Input vs. Temperature
CL = 5600pF, Vcc = 18V

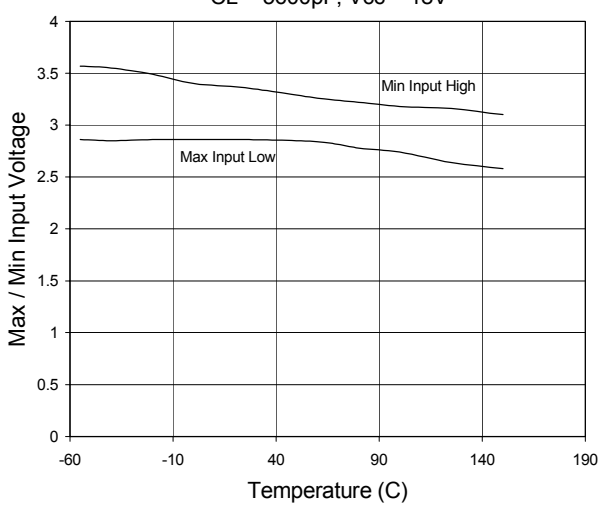


Fig. 9 Supply Current vs. Load Capacitance
Vcc = 13V

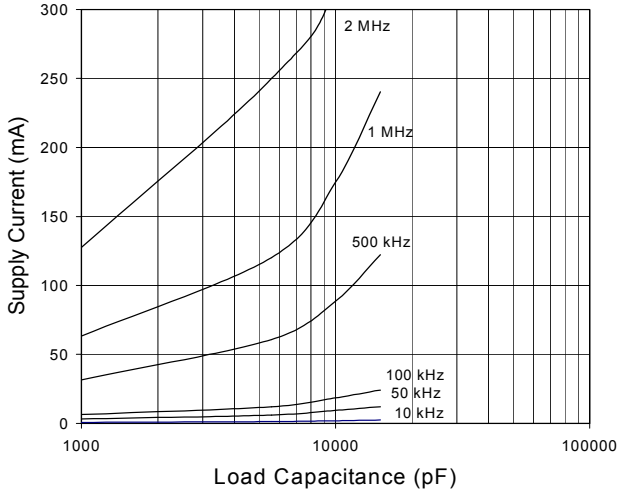


Fig. 10 Supply Current vs. Frequency
Vcc = 13V

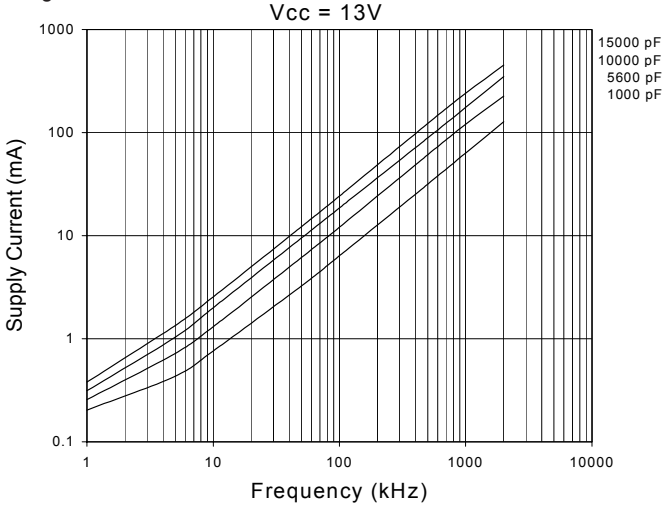


Fig. 11 Supply Current vs. Load Capacitance
Vcc = 18V

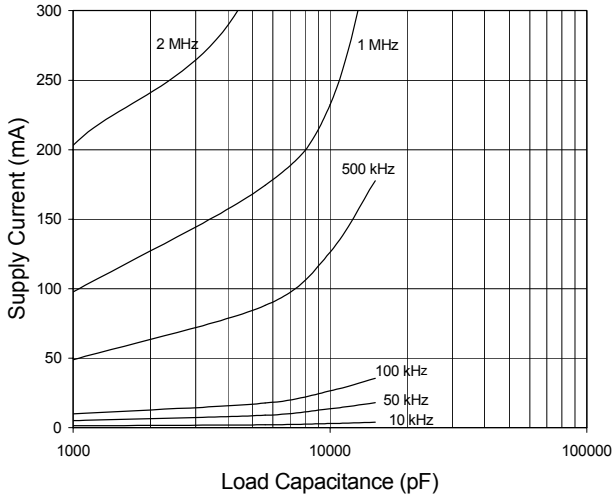


Fig. 12 Supply Current vs. Frequency
Vcc = 18V

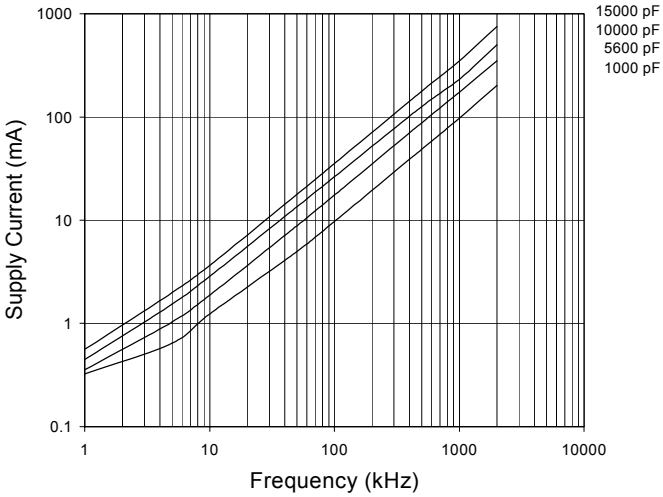


Fig. 13 Supply Current vs. Load Capacitance
Vcc = 25V

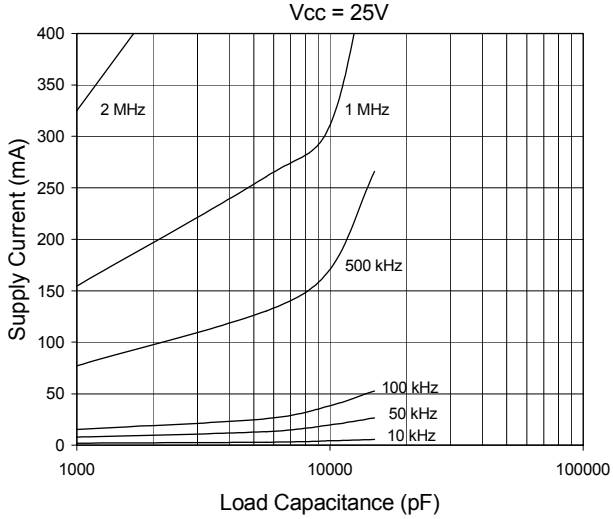


Fig. 14 Supply Current vs. Frequency
Vcc = 25V

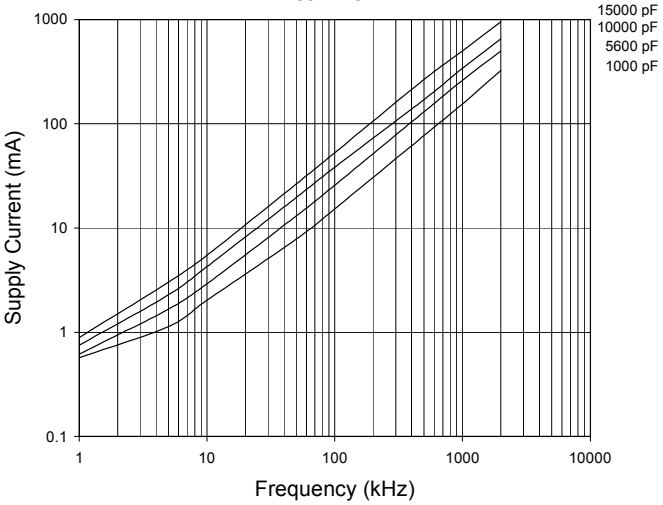


Fig. 15 Supply Current vs. Load Capacitance
Vcc = 35V

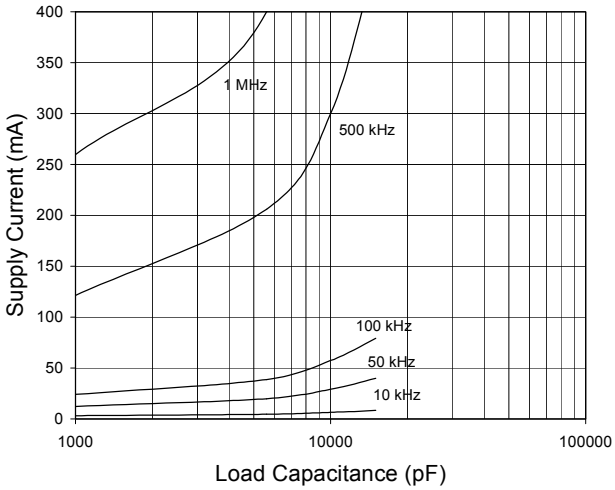


Fig. 16 Supply Current vs. Frequency
Vcc = 35V

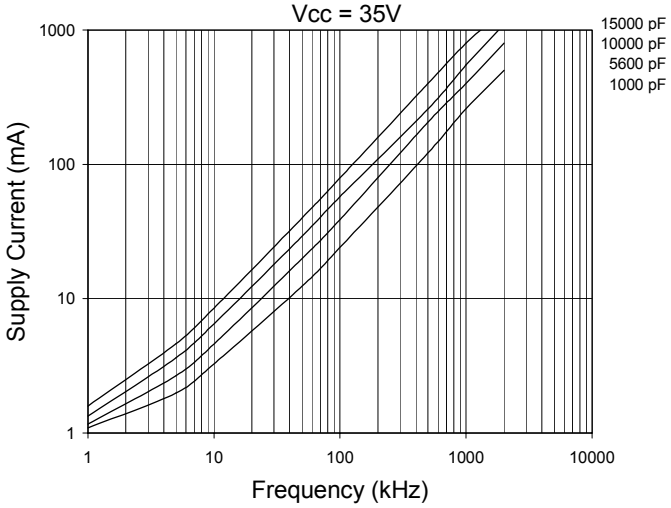


Fig. 17 Propagation Delay vs. Supply Voltage
C_L = 5600 pF Vin = 15V@1kHz

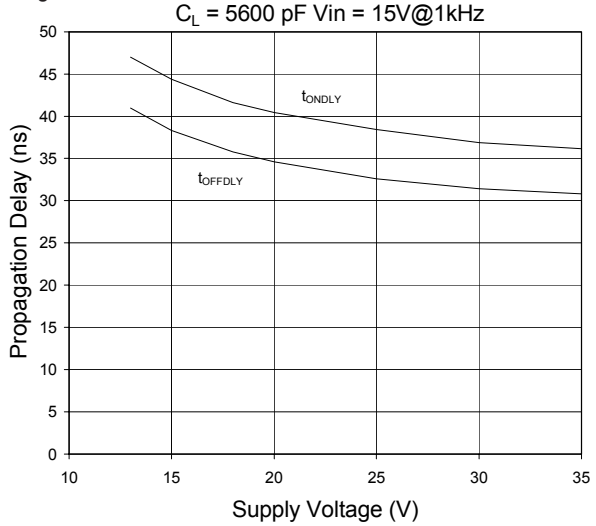


Fig. 18 Propagation Delay vs. Input Voltage
C_L = 5600 pF Vcc = 18V

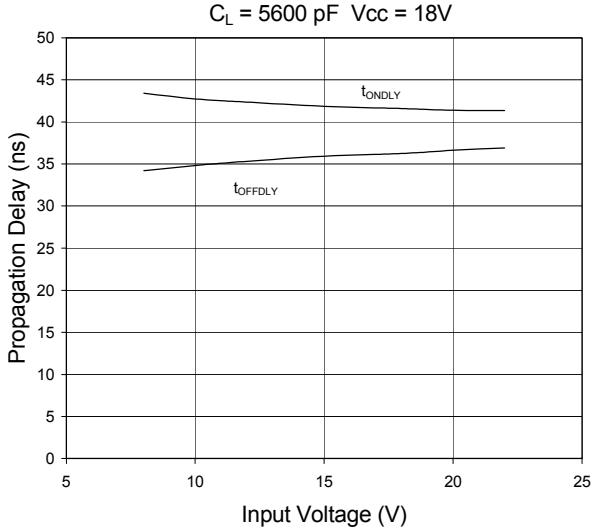


Fig. 19 Propagation Delay Times vs. Temperature
C_L = 5600pF, Vcc = 18V

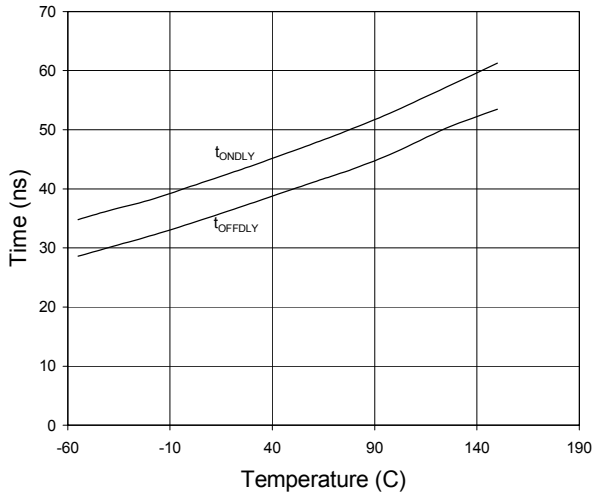


Fig. 20 Quiescent Supply Current vs. Temperature
Vcc = 18V, Vin = 15V@1kHz, C_L = 5600pF

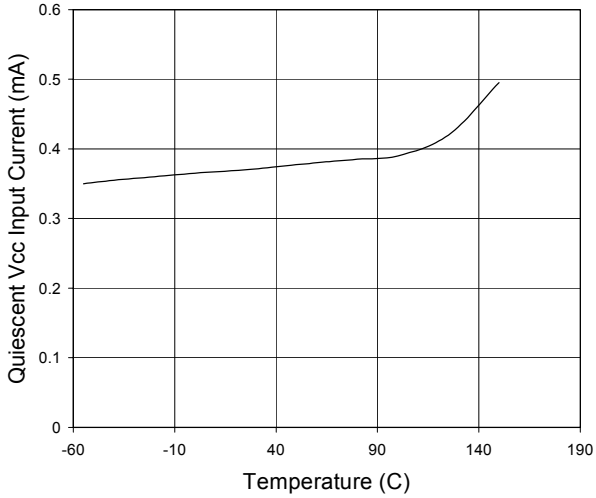


Fig. 21 High State Output Resistance vs. Supply Voltage

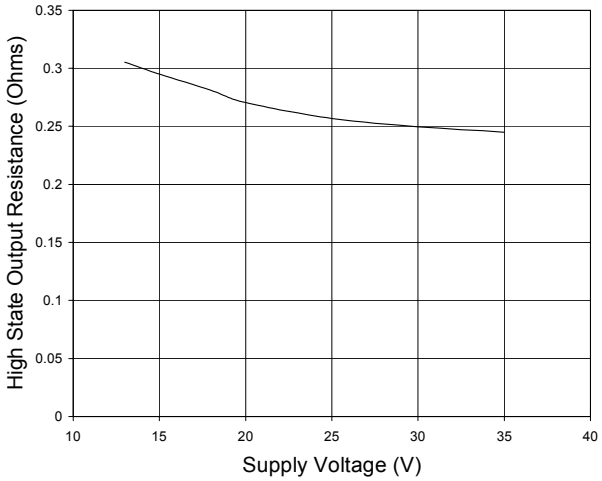


Fig. 22 Low State Output Resistance vs. Supply Voltage

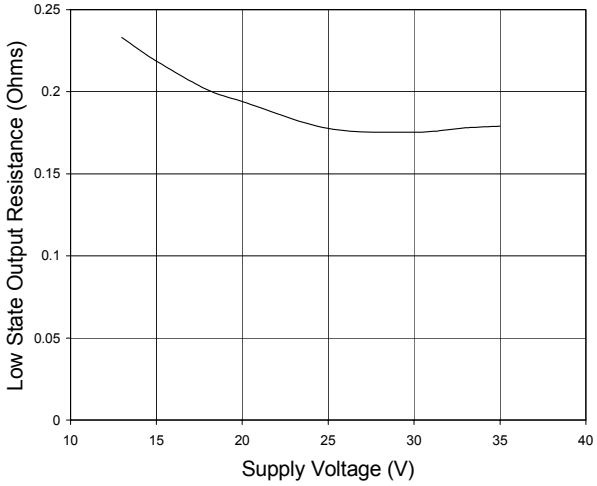


Fig. 23 P Channel Output Current vs. Vcc

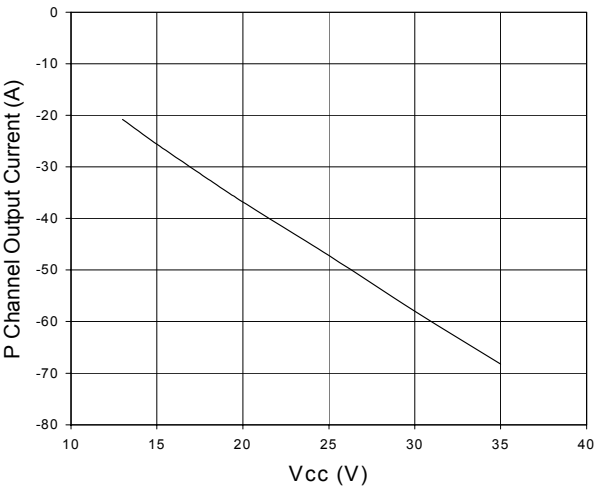


Fig. 24 N Channel Output Current vs. Vcc

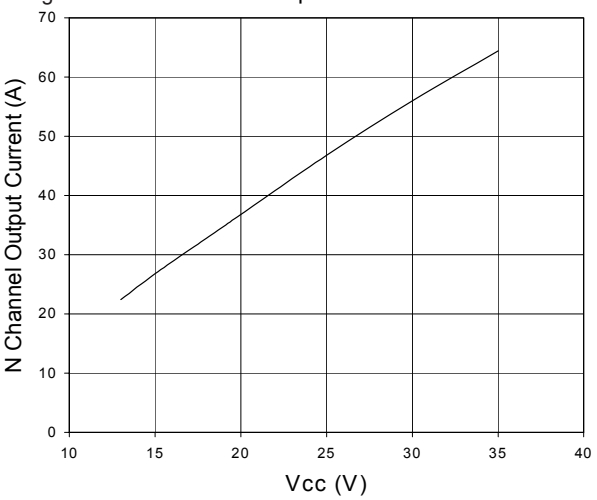


Fig. 25 P Channel Output Current vs. Temperature
Vcc = 18V

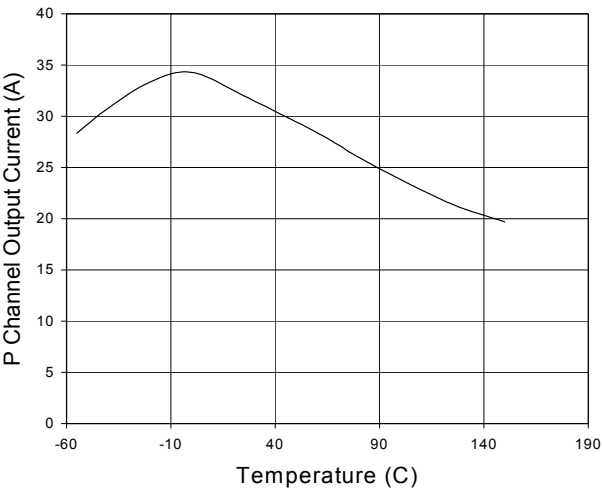


Fig. 26 N Channel Output Current vs. Temperature
Vcc = 18V

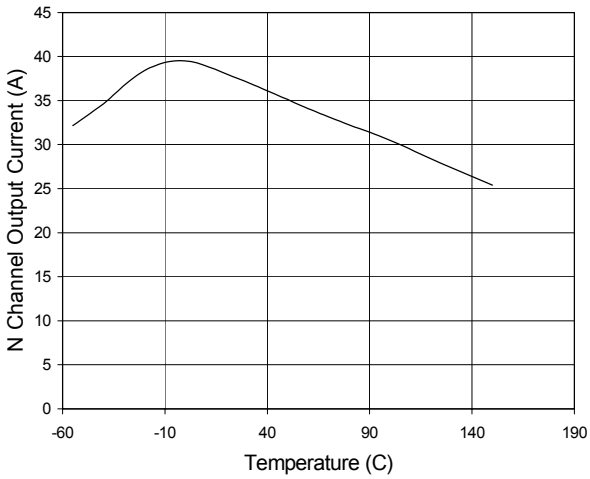


Figure 27 - Typical circuit to decrease di/dt during turn-off

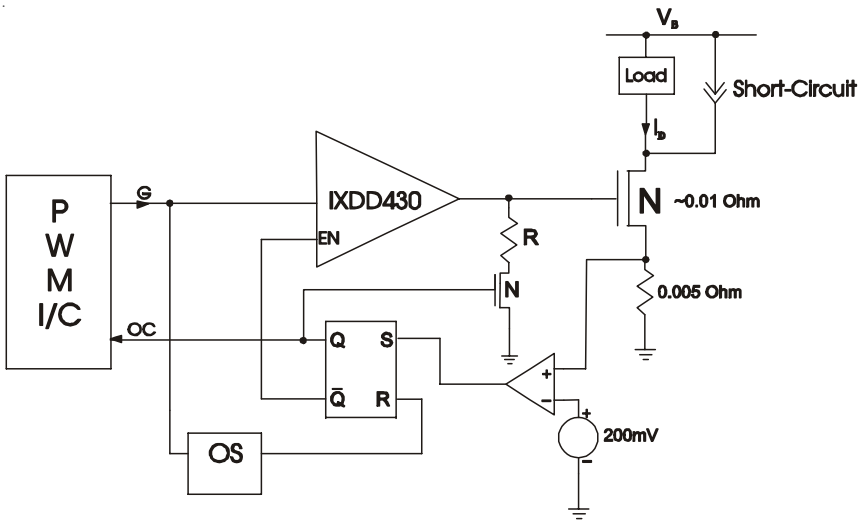
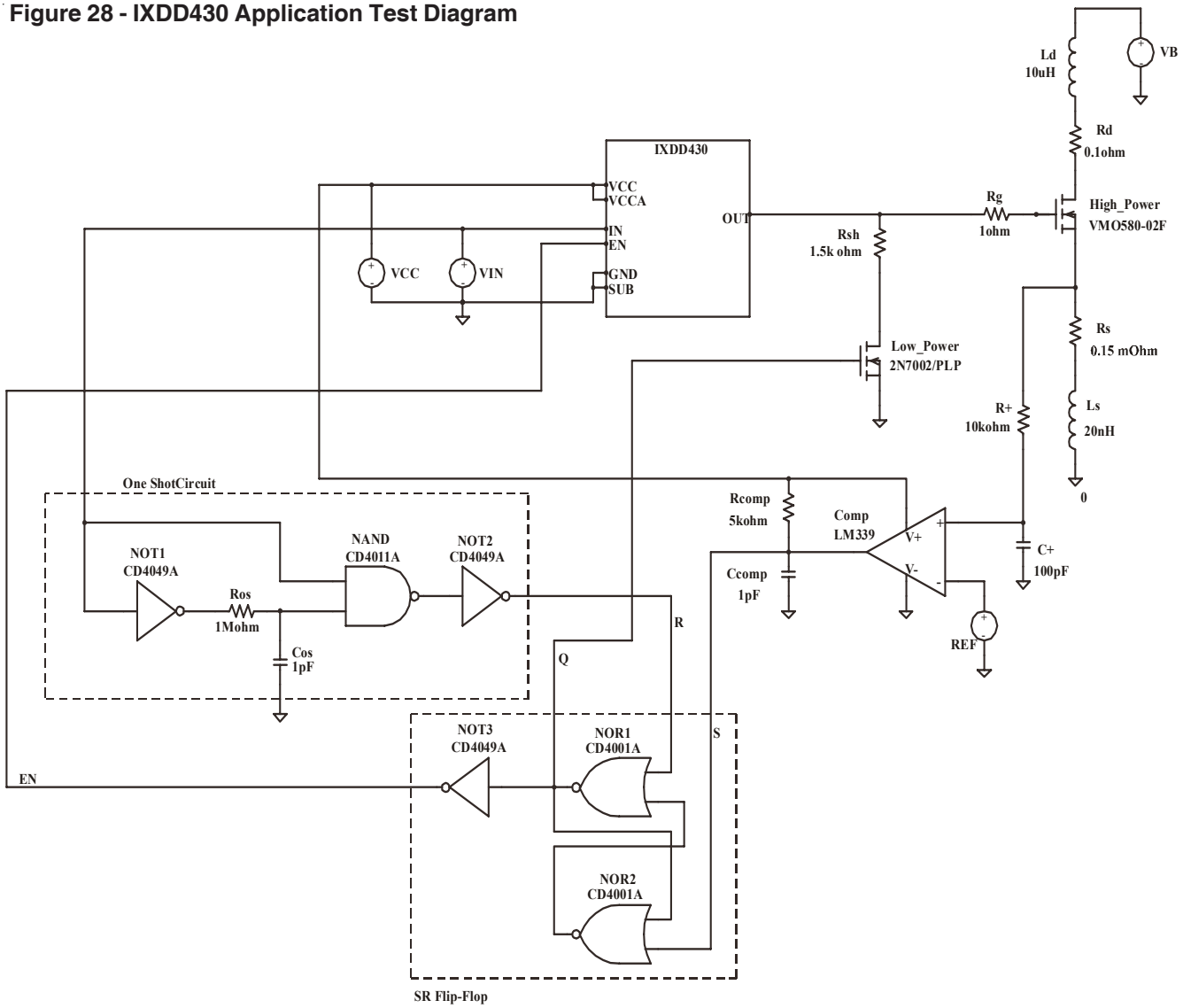


Figure 28 - IXDD430 Application Test Diagram



APPLICATIONS INFORMATION

Short Circuit di/dt Limit

A short circuit in a high-power MOSFET module such as the VM0580-02F, (580A, 200V), as shown in Figure 27, can cause the current through the module to flow in excess of 1500A for 10μs or more prior to self-destruction due to thermal runaway. For this reason, some protection circuitry is needed to turn off the MOSFET module. However, if the module is switched off too fast, there is a danger of voltage transients occuring on the drain due to Ldi/dt, (where L represents total inductance in series with drain). If these voltage transients exceed the MOSFET's voltage rating, this can cause an avalanche breakdown.

The IXDD430 has the unique capability to softly switch off the high-power MOSFET module, significantly reducing these Ldi/dt transients.

Thus, the IXDD430 helps to prevent device destruction from *both* dangers; over-current, and avalanche breakdown due to di/dt induced over-voltage transients.

The IXDD430 is designed to not only provide ±30A under normal conditions, but also to allow it's output to go into a high impedance state. This permits the IXDD430 output to control a separate weak pull-down circuit during detected overcurrent shutdown conditions to limit and separately control d_{VGS}/dt gate turnoff. This circuit is shown in Figure 28.

Referring to Figure 28, the protection circuitry should include a comparator, whose positive input is connected to the source of the VM0580-02. A low pass filter should be added to the input of the comparator to eliminate any glitches in voltage caused by the inductance of the wire connecting the source resistor to ground. (Those glitches might cause false triggering of the comparator).

The comparator's output should be connected to a SRFF(Set Reset Flip Flop). The flip-flop controls both the Enable signal, and the low power MOSFET gate. Please note that CMOS 4000-series devices operate with a V_{CC} range from 3 to 15 VDC, (with 18 VDC being the maximum allowable limit).

A low power MOSFET, such as the 2N7000, in series with a resistor, will enable the VMO580-02F gate voltage to drop gradually. The resistor should be chosen so that the RC time constant will be 100us, where "C" is the Miller capacitance of the VMO580-02F.

For resuming normal operation, a Reset signal is needed at the SRFF's input to enable the IXDD430 again. This Reset can be generated by connecting a One Shot circuit between the IXDD430 Input signal and the SRFF restart input. The One Shot will create a pulse on the rise of the IXDD430 input, and this pulse will reset the SRFF outputs to normal operation.

When a short circuit occurs, the voltage drop across the low-value, current-sensing resistor, (Rs=0.005 Ohm), connected between the MOSFET Source and ground, increases. This triggers the comparator at a preset level. The SRFF drives a low input into the Enable pin disabling the IXDD430 output. The SRFF also turns on the low power MOSFET, (2N7000).

In this way, the high-power MOSFET module is softly turned off by the IXDD430, preventing its destruction.

Supply Bypassing and Grounding Practices, Output Lead inductance

When designing a circuit to drive a high speed MOSFET utilizing the IXDD430/IXDI430/IXDN430, it is very important to keep certain design criteria in mind, in order to optimize performance of the driver. Particular attention needs to be paid to **Supply Bypassing**, **Grounding**, and minimizing the **Output Lead Inductance**.

Say, for example, we are using the IXDD430 to charge a 15nF capacitive load from 0 to 25 volts in 25ns.

Using the formula: $I = C \Delta V / \Delta t$, where ΔV=25V C=15nF & Δt=25ns we can determine that to charge 15nF to 25 volts in 25ns will take a constant current of 15A. (In reality, the charging current won't be constant, and will peak somewhere around 30A).

SUPPLY BYPASSING

In order for our design to turn the load on properly, the IXDD430 must be able to draw this 5A of current from the power supply in the 25ns. This means that there must be very low impedance between the driver and the power supply. The most common method of achieving this low impedance is to bypass the power supply at the driver with a capacitance value that is a magnitude larger than the load capacitance. Usually, this would be achieved by placing two different types of bypassing capacitors, with complementary impedance curves, very close to the driver itself. (These capacitors should be carefully selected, low inductance, low resistance, high-pulse current-service capacitors). Lead lengths may radiate at high frequency due to inductance, so care should be taken to keep the lengths of the leads between these bypass capacitors and the IXDD430 to an absolute minimum.

GROUNDING

In order for the design to turn the load off properly, the IXDD430 must be able to drain this 5A of current into an adequate grounding system. There are three paths for returning current that need to be considered: Path #1 is between the IXDD430 and it's load. Path #2 is between the IXDD430 and it's power supply. Path #3 is between the IXDD430 and whatever logic is driving it. All three of these paths should be as low in resistance and inductance as possible, and thus as short as practical. In addition, every effort should be made to keep these three ground paths distinctly separate. Otherwise, (for instance), the returning ground current from the load may develop a voltage that would have a detrimental effect on the logic line driving the IXDD430.

OUTPUT LEAD INDUCTANCE

Of equal importance to Supply Bypassing and Grounding are issues related to the Output Lead Inductance. Every effort should be made to keep the leads between the driver and it's load as short and wide as possible. If the driver must be placed farther than 2" from the load, then the output leads should be treated as transmission lines. In this case, a twisted-pair should be considered, and the return line of each twisted pair should be placed as close as possible to the ground pin of the driver, and connect directly to the ground terminal of the load.

TTL to High Voltage CMOS Level Translation (IXDD430 Only)

The enable (EN) input to the IXDD430 is a high voltage CMOS logic level input where the EN input threshold is ½ V_{CC}, and may not be compatible with 5V CMOS or TTL input levels. The IXDD430 EN input was intentionally designed for enhanced noise immunity with the high voltage CMOS logic levels. In a typical gate driver application, V_{CC} =15V and the EN input threshold at 7.5V, a 5V CMOS logical high input applied to this typical IXDD430 application's EN input will be misinterpreted as a logical low, and may cause undesirable or unexpected results. The note below is for optional adaptation of TTL or 5V CMOS levels.

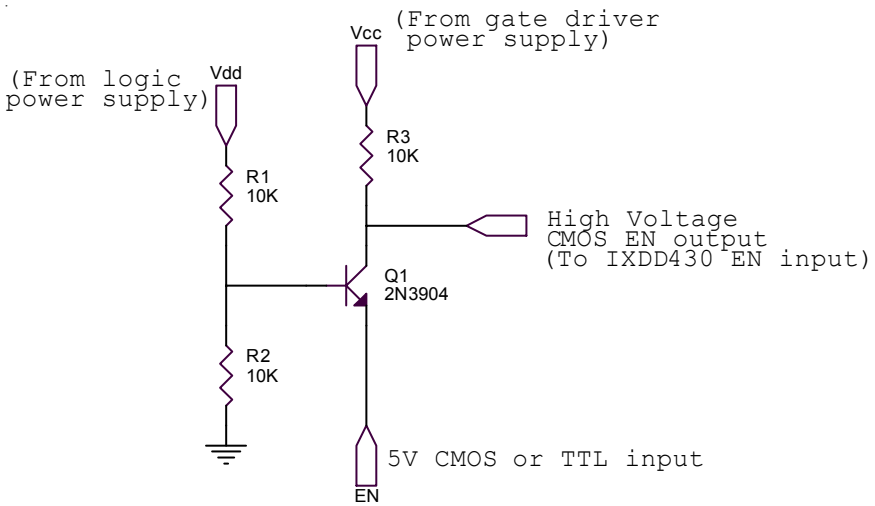
The circuit in Figure 29 alleviates this potential logic level misinterpretation by translating a TTL or 5V CMOS logic input to high voltage CMOS logic levels needed by the IXDD430 EN input. From the figure, V_{CC} is the gate driver power supply, typically set between 8V to 20V, and V_{DD} is the logic power supply, typically between 3.3V to 5.5V. Resistors R1 and R2 form a voltage divider network so that the Q1 base is positioned at the midpoint of the expected TTL logic transition levels.

A TTL or 5V CMOS logic low, V_{TTLLOW}=~<0.8V, input applied to the Q1 emitter will drive it on. This causes the level translator output, the Q1 collector output to settle to $V_{CESATQ1}$ + V_{TTLLOW}=<~2V, which is sufficiently low to be correctly interpreted as a high voltage CMOS logic low (<1/3V_{CC}=5V for V_{CC} =15V given in the IXDD430 data sheet.)

A TTL high, $V_{TTLHIGH}$=>~2.4V, or a 5V CMOS high, $V_{5VCMOSHIGH}$=~>3.5V, applied to the EN input of the circuit in Figure 29 will cause Q1 to be biased off. This results in Q1 collector being pulled up by R3 to V_{CC}=15V, and provides a high voltage CMOS logic high output. The high voltage CMOS logical EN output applied to the IXDD430 EN input will enable it, allowing the gate driver to fully function as an 30 Amp output driver.

The total component cost of the circuit in Figure 29 is less than $0.10 if purchased in quantities >1K pieces. It is recommended that the physical placement of the level translator circuit be placed close to the source of the TTL or CMOS logic circuits to maximize noise rejection.

Figure 29 - TTL to High Voltage CMOS Level Translator



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