HD14549B, HD14559B

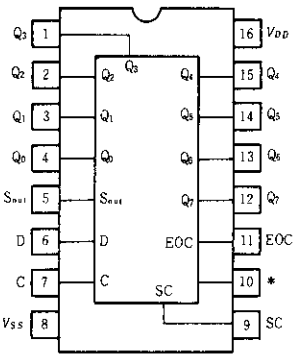
Successive Approximation Register

The HD14549B and the HD14559B successive approximation registers are 8-bit registers providing all the digital control and storage necessary for successive approximation analog-to-digital conversion systems. These parts differ in only one control input. The Master Reset (MR) on the HD14549B is required in the cascaded mode when greater than 8 bits are disired. The Feed Forward (FF) of the HD14559B is used for register shortening where End-of-Conversion (EOC) is required after less than eight cycles. Applications for the HD14549B and HD14559B include analog-to-digital conversion, with serial and parallel outputs

■ FEATURES

- Totally Synchronous Operation
- All Outputs Buffered
- Single Supply Operation
- Serial Output
- Retriggerable
- Compatible with a Variety of Digital and Analog Systems such as the HA17408P 8-bit D/A Converter
- All Control Inputs Positive-Edge Triggered
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range

■ PIN ARRANGEMENT



(Top View)

Note) * : HD14549B is MR input.
HD14559B is FF input.

■ TRUTH TABLE

● HD14549B

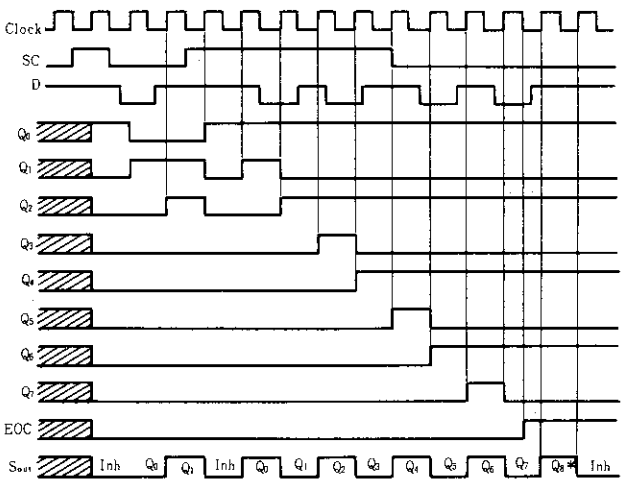
SC	$SC_{(t-1)}$	MR	$MR_{(t-1)}$	Clock	Action
×	×	×	×	↓	
×	×	1	×	↑	Reset
1	0	0	0	↑	Start Conversion
1	×	0	1	↑	Start Conversion
1	1	0	0	↑	Continue Conversion
0	×	0	×	↑	Continue Previous Operation

× = Don't Care
t-1 = State at Previous Clock ↑

● HD14559B

SC	$SC_{(t-1)}$	EOC	Clock	Action
×	×	×	↓	
1	0	0	↑	Start Conversion
×	1	0	↑	Continue Conversion
0	0	0	↑	Continue Conversion
0	×	1	↑	Retain Conversion Result
1	×	1	↑	Start Conversion

■ TIMING DIAGRAM



Note) ▨ ; Don't care condition
Inh ; Indicates Serial Out is inhibited low.
* ; Q_8 is ninthbit of serial information available from 8-bit register.
Pin 10 = V_{SS}

■ ELECTRICAL CHARACTERISTICS

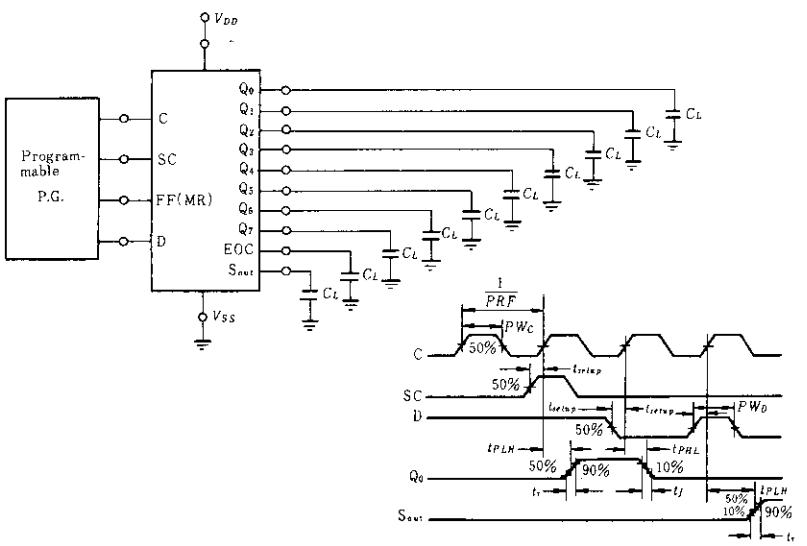
Characteristic		Symbol	V_{DD}(V)	Test Conditions	−40°C min	−40°C max	25°C min	25°C typ	25°C max	85°C min	85°C max	Unit
Output Voltage		V_{OL}	5.0	V_{in} = V_{DD} or 0	—	0.05	—	0	0.05	—	0.05	V
			10		—	0.05	—	0	0.05	—	0.05	
			15		—	0.05	—	0	0.05	—	0.05	
		V_{OH}	5.0	V_{in} = 0 or V_{DD}	4.95	—	4.95	5.0	—	4.95	—	V
			10		9.95	—	9.95	10	—	9.95	—	
			15		14.95	—	14.95	15	—	14.95	—	
Input Voltage		V_{IL}	5.0	V_{out} = 4.5 or 0.5V	—	1.5	—	2.25	1.5	—	1.5	V
			10	V_{out} = 9.0 or 1.0V	—	3.0	—	4.50	3.0	—	3.0	
			15	V_{out} = 13.5 or 1.5V	—	4.0	—	6.75	4.0	—	4.0	
		V_{IH}	5.0	V_{out} = 0.5 or 4.5V	3.5	—	3.5	2.75	—	3.5	—	V
			10	V_{out} = 1.0 or 9.0V	7.0	—	7.0	5.50	—	7.0	—	
			15	V_{out} = 1.5 or 13.5V	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current		I_{OH}	5.0	V_{OH} = 2.5V	−1.0	—	−0.8	−1.7	—	−0.6	—	mA
			5.0	V_{OH} = 4.6V	−0.2	—	−0.16	−0.36	—	−0.12	—	
			10	V_{OH} = 9.5V	−0.5	—	−0.4	−0.9	—	−0.3	—	
			15	V_{OH} = 13.5V	−1.4	—	−1.2	−3.5	—	−1.0	—	
	Q	I_{OL}	5.0	V_{OL} = 0.4V	1.04	—	0.88	1.76	—	0.72	—	mA
			10	V_{OL} = 0.5V	2.6	—	2.2	4.5	—	1.8	—	
			15	V_{OL} = 1.5V	7.2	—	6.0	17.6	—	4.8	—	
	Pin 5, 11		5.0	V_{OL} = 0.4V	0.52	—	0.44	0.88	—	0.36	—	
			10	V_{OL} = 0.5V	1.3	—	1.1	2.25	—	0.9	—	
			15	V_{OL} = 1.5V	3.6	—	3.0	8.8	—	2.4	—	
Input Current		I_{in}	15		—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance		C_{in}		V_{in} = 0	—	—	—	5.0	7.5	—	—	pF
Quiescent Current		I_{DD}	5.0	Zero Signal, per Package	—	20	—	0.005	20	—	150	μA
			10		—	40	—	0.010	40	—	300	
			15		—	80	—	0.015	80	—	600	
Total Supply Current*		I_T	5.0	Dynamic + I_{DD}, per Gate C_L = 50pF, f = 1kHz	—	—	—	0.8	—	—	—	μA
			10		—	—	—	1.6	—	—	—	
			15		—	—	—	2.4	—	—	—	

* To calculate total supply current at frequency other than 1kHz.
@V_{DD} = 5.0V I_T = (0.8 μA/kHz)f + I_{DD}, @V_{DD} = 10V I_T = (1.6 μA/kHz)f + I_{DD}, @V_{DD} = 15V I_T = (2.4 μA/kHz)f + I_{DD}

■ SWITCHING CHARACTERISTICS (C_L=50pF, Ta=25°C)

Characteristic		Symbol	V_{DD}(V)	min	typ	max	Unit
Output Rise Time		t_r	5.0	—	180	400	ns
			10	—	90	200	
			15	—	65	160	
Output Fall Time		t_f	5.0	—	120	250	ns
			10	—	60	125	
			15	—	40	100	
Propagation Delay Time	Clock to Q	t_{PLH}, t_{PHL}	5.0	—	500	1200	ns
			10	—	210	500	
			15	—	155	380	
	Clock to Sout		5.0	—	750	1800	
			10	—	310	750	
			15	—	220	550	
	Clock to EOC		5.0	—	300	750	
			10	—	130	325	
			15	—	100	250	
SC, D, FF, MR Setup Time		t_{setup}	5.0	300	125	—	ns
			10	150	50	—	
			15	115	40	—	
Clock Pulse Width		PW_C	5.0	600	350	—	ns
			10	300	135	—	
			15	225	100	—	
D, SC, FF, MR Pulse Width		PW	5.0	750	250	—	ns
			10	300	100	—	
			15	225	80	—	
Clock Pulse Rise and Fall Time		t_r, t_f	5.0	—	—	15	μs
			10	—	—	5.0	
			15	—	—	4.0	
Clock Frequency		PRF	5.0	—	1.5	0.8	MHz
			10	—	3.0	1.5	
			15	—	4.0	2.0	

■ SWITCHING TIME TEST CIRCUIT



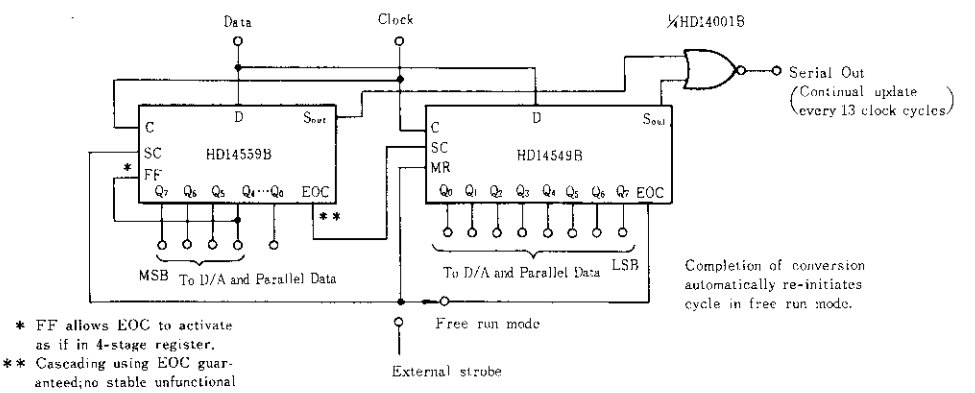
Note : Pin 10=V_{SS}

■ OPERATING CHARACTERISTICS

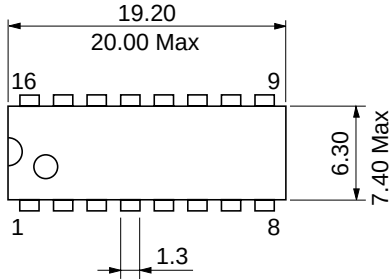
Both the HD14549B and HD14559B can be operated in either the "free run" or "strobed operation" mode for conversion schemes with any number of bits. Reliable cascading and/or recirculating operation can be achieved if the End of Convert (EOC) output is used as the controlling function, since with EOC = 0 (and with SC = 1 for HD14549B but either 1 or 0 for HD14559B) no stable state exists under continual clocked operation. The HD14559B will automatically recirculate after EOC = 1 during externally strobed operation, provided SC = 1. All data and control inputs for these devices are triggered into the circuit on the positive edge of the clock pulse. Operation of the various terminals is as follows:

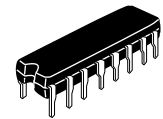
- C = Clock ... A Positive-going transition of the Clock is required for data on any input to be strobed into the circuit.
- SC = Start Convert ... A conversion sequence is initiated on the positive-going transition of the SC input on succeeding clock cycles.
- D = Data In ... Data on this input (usually from a comparator in A/D applications) is also entered into the circuit on a positive-going transition of the clock. This input is Schmitt triggered and synchronized to allow fast response and guaranteed quality of serial and parallel data.
- MR = Master Reset (HD14549B only) ... Resets all output to 0 on positive-going transitions of the clock, if removed while SC = 0, the circuit will remain reset until SC = 1. This allow easy cascading of circuits.
- FF = Feed Forward (HD14559B only) ... Provides register shortening by removing unwanted bits from a system. For operation with less than 8 bits, tie the output following the least significant bit of the circuits to EOC. E. G., for a 6-bit conversion, tie Q1 to FF; the part will respond as shown in the timing diagram less two bit times. Not that Q1 and Q0 will still operate and must be disregarded. For 8-bit operation, FF is tied to V_{SS}. For applications with more than 8 but less than 16 bits, use the basic connections shown in Figure 1. The FF input of the HD14559B is used to shorten the setup. Tying FF directly to the least significant bit used in the HD14559B allows EOC to provide the cascading signal, and results in smooth transition of serial information from the HD14559B to the HD14549B. The Serial Out (Sout) inhibit structure of the HD14559B remains inactive one cycle after EOC goes high, while Sout of the HD14549B remains inhibited until the second clock cycle of its operation.
- Qn = Data Outputs ... After a conversion is initiated the Q's on succeeding cycles go high and are then conditionally reset dependent upon the state of the D input. Once conditionally reset they remain in the proper state until the circuit is either reset or reinitiated.
- EOC = End of Convert ... This output goes high on the negative-going transition of the clock following FF = 1 (for the HD14559B) or the conditional reset of Q0. This allows settling of the digital circuitry prior to the End of Conversion indication. Therefore either level or edge triggering can indicate complete conversion.
- Sout = Serial Out ... Transmits conversion in serial fashion. Serial data occurs during the clock period when the corresponding parallel data bit is conditionally reset. Serial Out is inhibited on the initial period of a cycle, when the circuit is reset, and on the second cycle after EOC goes high. This provides efficient operation when cascaded.

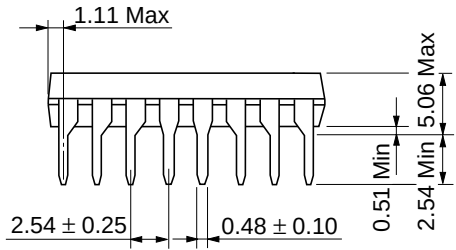
●12-bit Conversion Scheme

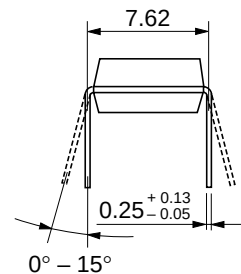


Unit: mm









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