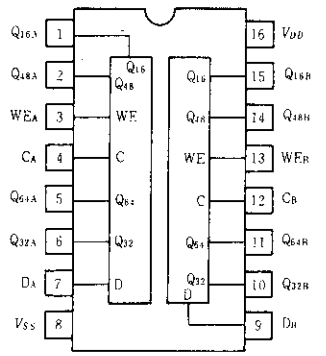
Dual 64-bit Static Shift Register

The HD14517B dual 64-bit static shift register consists of two identical, independent, 64-bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48 and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16-bit, 32-bit, and 48-bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods, and also permits bus logic to be used. This device is useful in time delay circuits, temporary memory storage circuits, and other serial shift register applications.

■ PIN ARRANGEMENT

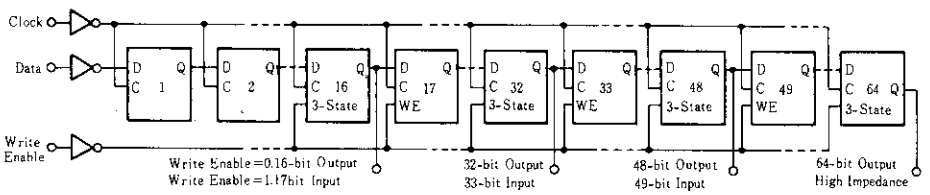


(Top View)

■ FEATURES

- Quiescent Current = 10nA/pkg typ. @5V
- Noise Immunity of V_{DD} typ.
- Fully Static Operation
- Output Transitions Occur on the Rising Edge of the Clock Pulse
- 6.7MHz Operation @10V
- Exceedingly Slow Input Transition Rates May Be Apolied to the Clock Input
- 3-state Output at 64th-bit Allows Use in Bus Logic Applications
- Shift Registers of any Length may be Fully Loaded with 16 Clock Pulses
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range

■ BLOCK DIAGRAM (1/2)



■ TRUTH TABLE

Clock	Write Enable	Data	16-bit Tap	32-bit Tap	48-bit Tap	64-bit Tap
0	0	×	Content of 16-bit Displayed	Content of 32-bit Displayed	Content of 48-bit Displayed	Content of 64-bit Displayed
0	1	×	High Impedance	High Impedance	High Impedance	High Impedance
1	0	×	Content of 16-bit Displayed	Content of 32-bit Displayed	Content of 48-bit Displayed	Content of 64-bit Displayed
1	1	×	High Impedance	High Impedance	High Impedance	High Impedance
⎍	0	Data entered into 1st Bit	Content of 16-bit Displayed	Content of 32-bit Displayed	Content of 48-bit Displayed	Content of 64-bit Displayed
⎍	1	Data entered into 1st Bit	Data at tap entered into 17-bit	Data at tap entered into 33-bit	Data at tap entered into 49-bit	High Impedance
⎍	0	×	Content of 16-bit Displayed	Content of 32-bit Displayed	Content of 48-bit Displayed	Content of 64-bit Displayed
⎍	1	×	High Impedance	High Impedance	High Impedance	High Impedance

x=Don't Care

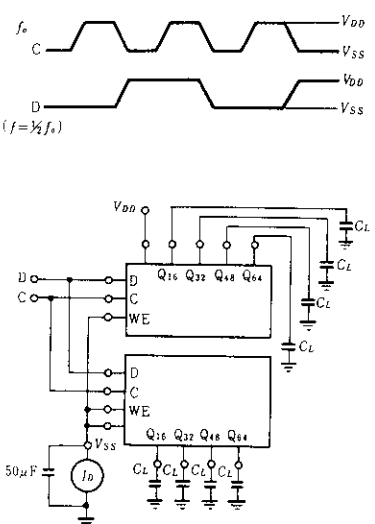
■ ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}(V)	Test Conditions	−40°C min	−40°C max	25°C min	25°C typ	25°C max	85°C min	85°C max	Unit
Output Voltage	V_{OL}	5.0	$V_{in}=V_{DD}$ or 0	—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	V_{OH}	5.0	$V_{in}=0$ or V_{DD}	4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	V_{IL}	5.0	$V_{out}=4.5$ or 0.5V	—	1.5	—	2.25	1.5	—	1.5	V
		10	$V_{out}=9.0$ or 1.0V	—	3.0	—	4.50	3.0	—	3.0	
		15	$V_{out}=13.5$ or 1.5V	—	4.0	—	6.75	4.0	—	4.0	
	V_{IH}	5.0	$V_{out}=0.5$ or 4.5V	3.5	—	3.5	2.75	—	3.5	—	V
		10	$V_{out}=1.0$ or 9.0V	7.0	—	7.0	5.50	—	7.0	—	
		15	$V_{out}=1.5$ or 13.5V	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I_{OH}	5.0	$V_{OH}=2.5$V	−1.0	—	−0.8	−1.7	—	−0.6	—	mA
		5.0	$V_{OH}=4.6$V	−0.2	—	−0.16	−0.36	—	−0.12	—	
		10	$V_{OH}=9.5$V	−0.5	—	−0.4	−0.9	—	−0.3	—	
		15	$V_{OH}=13.5$V	−1.4	—	−1.2	−3.5	—	−1.0	—	
	I_{OL}	5.0	$V_{OL}=0.4$V	0.52	—	0.44	0.88	—	0.36	—	mA
		10	$V_{OL}=0.5$V	1.3	—	1.1	2.25	—	0.9	—	
		15	$V_{OL}=1.5$V	3.6	—	3.0	8.8	—	2.4	—	
Input Current	I_{in}	15		—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance	C_{in}		$V_{in}=0$	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD}	5.0	Zero Signal, per Package	—	50	—	0.010	50	—	375	μA
		10		—	100	—	0.020	100	—	750	
		15		—	200	—	0.030	200	—	1500	
Total Supply Current*	I_T	5.0	Dynamic+I_{DD}, per Gate $C_L=50$pF, $f=1$ kHz	—	—	—	4.2	—	—	—	μA
		10		—	—	—	8.8	—	—	—	
		15		—	—	—	13.7	—	—	—	
Three-State Output Leakage Current	I_{TL}	15		—	±1.0	—	±0.00001	±1.0	—	±7.5	μA

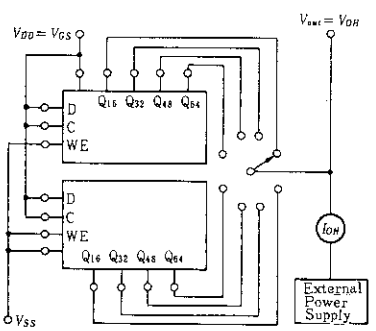
* To calculate total supply current at frequency other than 1kHz.
@$V_{DD}=5.0$V $I_T=(4.2\,\mu A/kHz)f+I_{DD}$, @$V_{DD}=10$V $I_T=(8.8\,\mu A/kHz)f+I_{DD}$, @$V_{DD}=15$V $I_T=(13.7\,\mu A/kHz)f+I_{DD}$

■ DC CHARACTERISTIC TEST CIRCUIT

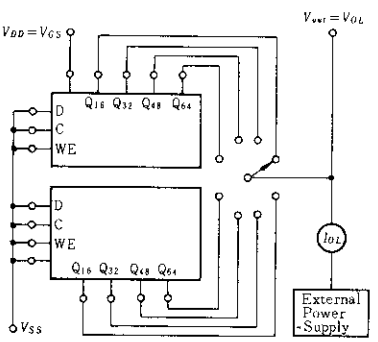
■ POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



● I_{OH}



● I_{OL}

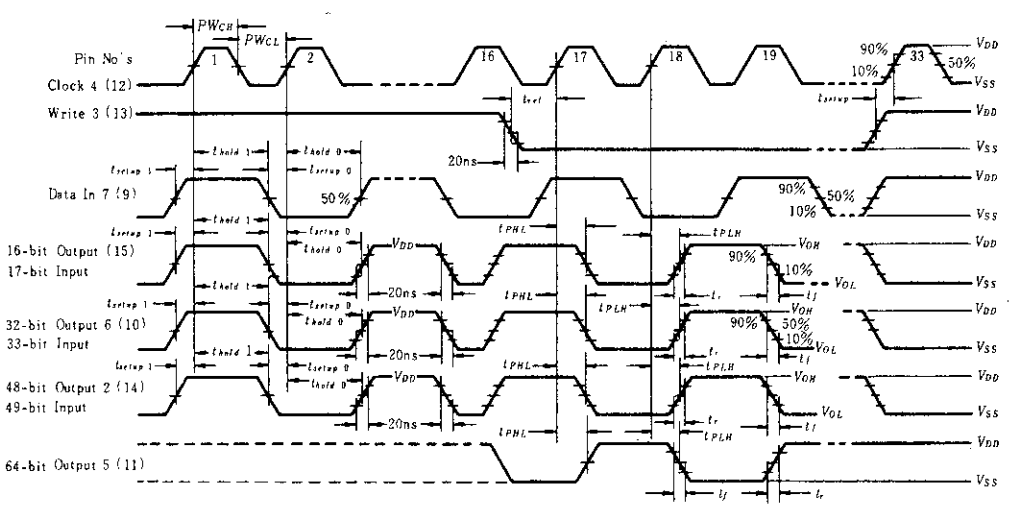


■SWITCHING CHARACTERISTICS (C_L=50pF, Ta=25°C)

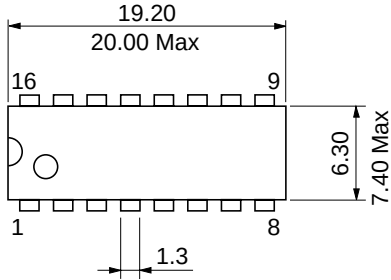
Characteristic	Symbol	V_{DD}(V)	min	typ	max	Unit
Output Rise Time	t_r	5.0	—	180	400	ns
		10	—	90	200	
		15	—	65	160	
Output Fall Time	t_f	5.0	—	100	200	ns
		10	—	50	100	
		15	—	37	80	
Propagation Delay Time	t_{PLH}, t_{PHL}	5.0	—	475	770	ns
		10	—	210	300	
		15	—	140	215	
Clock Pulse Width	PW_C	5.0	330	170	—	ns
		10	125	75	—	
		15	100	60	—	
Clock Frequency	PRF	5.0	—	3.0	1.5	MHz
		10	—	6.7	4.0	
		15	—	8.3	5.3	
Clock Pulse Rise and Fall Time	t_r, t_f	5.0	*			
		10				
		15				
Setup Time	t_{setup}	5.0	0	−40	—	ns
		10	10	−15	—	
		15	15	0	—	
Hold Time	t_{hold}	5.0	150	75	—	ns
		10	75	25	—	
		15	35	10	—	
Write Enable to Clock Setup Time	t_{setup}	5.0	400	170	—	ns
		10	200	65	—	
		15	110	50	—	
Write Enable to Clock Release Time	t_{rel}	5.0	380	160	—	ns
		10	180	55	—	
		15	100	40	—	

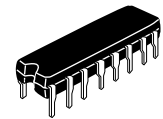
*When shift register sections are cascaded, the maxmum rise and fall time of the clock input should be equal to or less than the rise and fall time of the data outputs, driving data inputs, plus the propagation delay of the output driving stage.

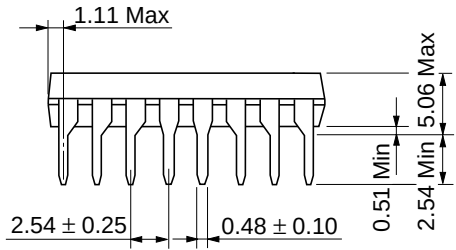
●DYNAMIC SIGNAL WAVEFORMS

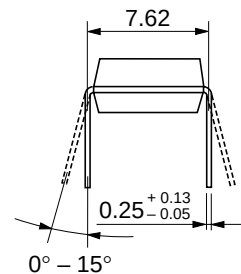


Unit: mm









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