TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

2SK1061

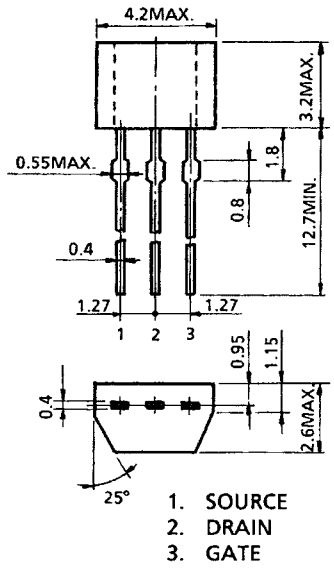
High Speed Switching Applications
Analog Switch Applications
Interface Applications

- Excellent switching times: t_{on} = 14 ns (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 100 mS (min)
- Low on resistance: $R_{DS\ (ON)}$ = 0.6 Ω (typ.)
- Enhancement-mode
- Complementary to 2SJ167

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DS}	60	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC	I_D	200	mA
	Pulse	I_{DP}	800	
Drain power dissipation (Ta = 25°C)		P_D	300	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

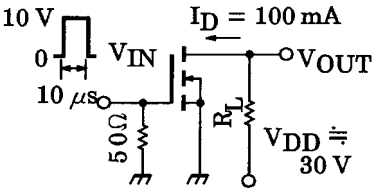
Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-4E1E

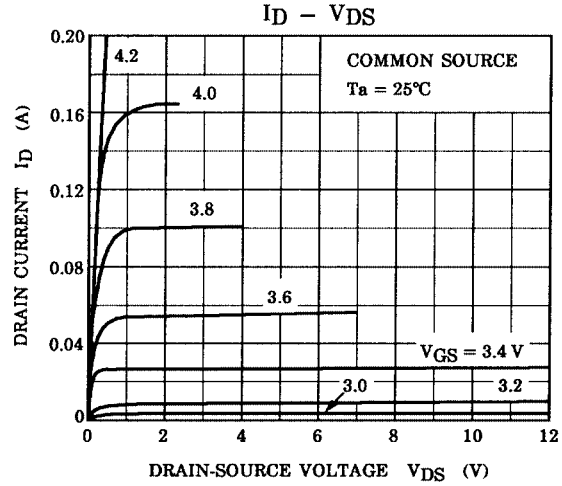
Weight: 0.13 g (typ.)

Electrical Characteristics (Ta = 25°C)

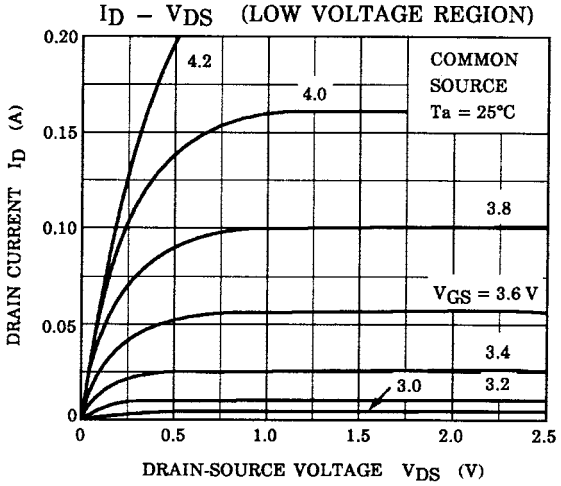
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	—	±100	nA
Drain cut-off current		I_{DSS}	V_{DS} = 60 V, V_{GS} = 0	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 1 mA, V_{GS} = 0	60	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	2	—	3.5	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 50 mA	100	—	—	mS
Drain-source ON resistance		$R_{DS\ (ON)}$	I_D = 50 mA, V_{GS} = 10 V	—	0.6	1.0	Ω
Drain-source ON voltage		$V_{DS\ (ON)}$	I_D = 50 mA, V_{GS} = 10 V	—	30	50	mV
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	—	55	65	pF
Reverse transfer capacitance		C_{rss}		—	13	18	pF
Output capacitance		C_{oss}		—	40	50	pF
Switching time	Rise time	t_r	 D.U. ≦ 1% V_{IN}: t_r, t_f < 5 ns (Z_{out} = 50 Ω)	—	8	—	ns
	Turn-on time	t_{on}		—	14	—	
	Fall time	t_f		—	35	—	
	Turn-off Time	t_{off}		—	75	—	

Note: This transistor is the electrostatic sensitive device. Please handle with caution.

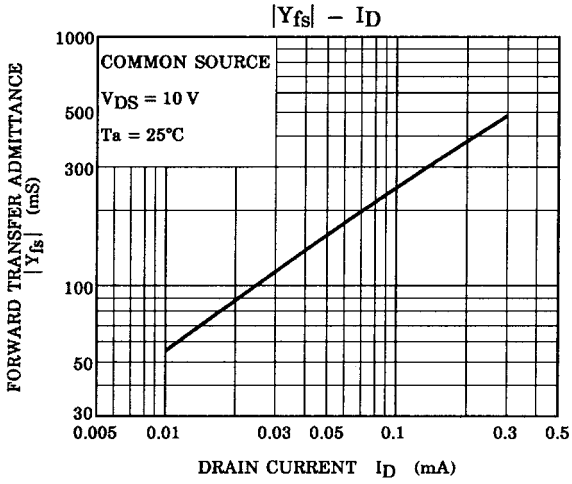
$I_D - V_{DS}$



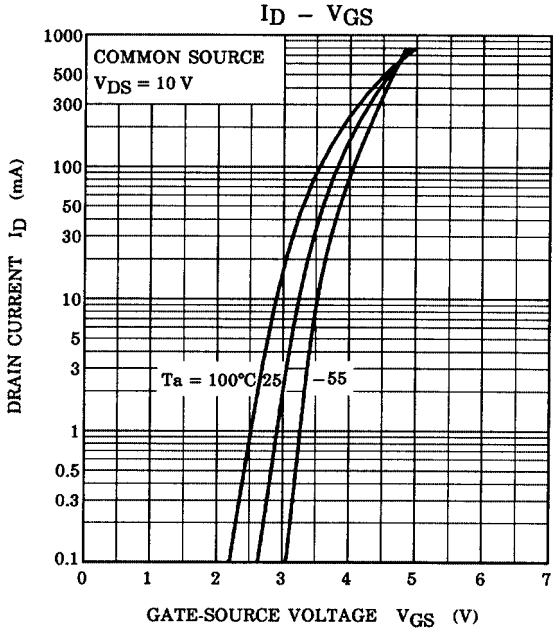
$I_D - V_{DS}$ (LOW VOLTAGE REGION)



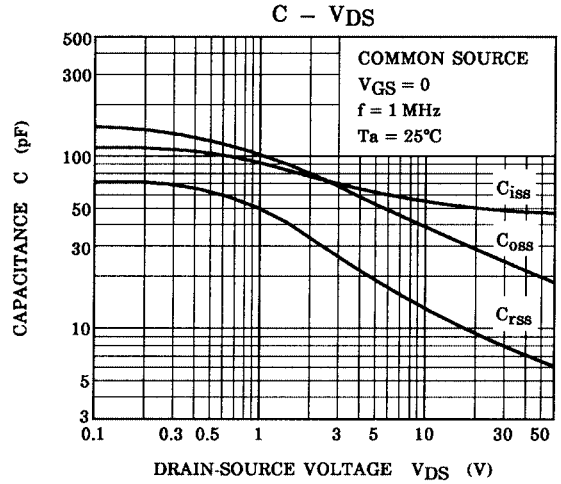
$|Y_{fs}| - I_D$



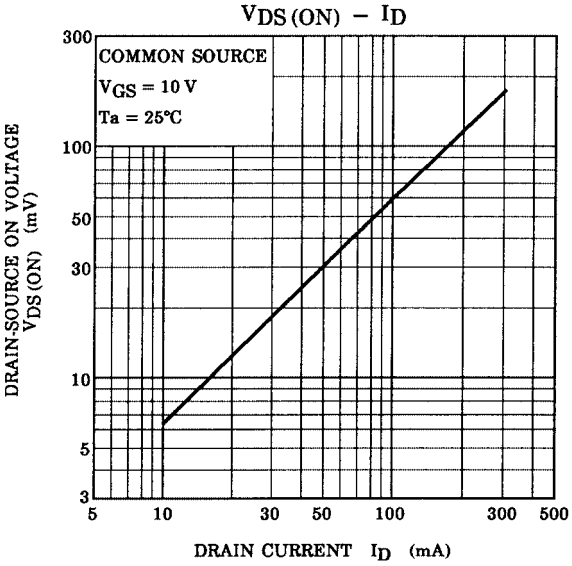
$I_D - V_{GS}$



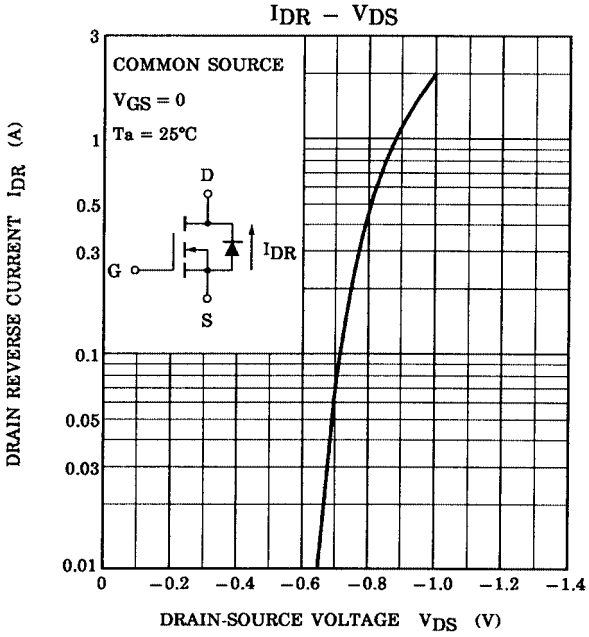
$C - V_{DS}$



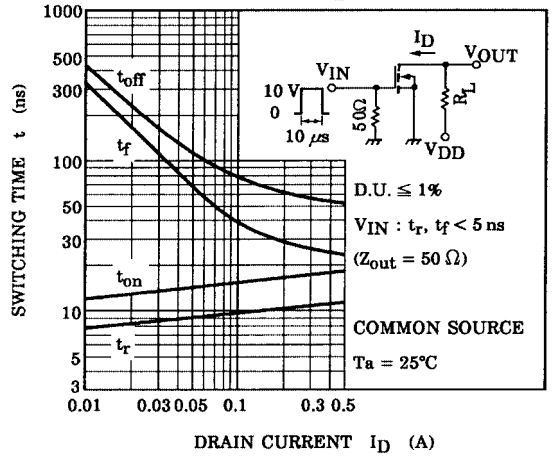
$V_{DS\,(ON)}$ – I_D



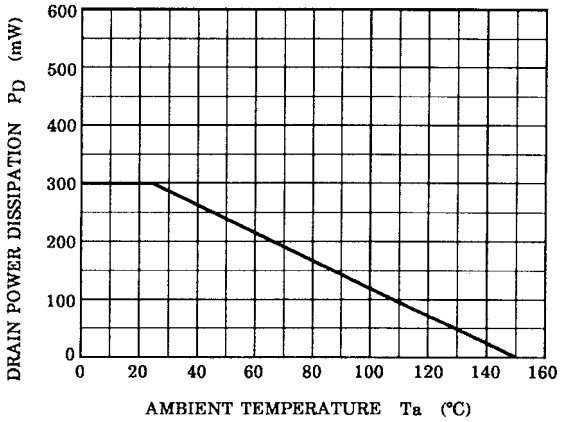
I_{DR} – V_{DS}



t – I_D



P_D – Ta



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